outline

1	about entrepreneurship	20/06	JEF
2	semiconductor industry	27/06	JMM
3	a-to-z of startup creation (1)	04/07	JEF
4	a-to-z of startup creation (2)	11/07	JEF
5	Engaging in business	18/07	JMM
6	let’s pitch and discuss	25/07	

outline

- 2 the semiconductor industry 27/06 JMM
  - a overview of the semiconductor value chain
  - b value creation across the value chain
  - c design-based business models
  - d competitive opportunities

Semiconductors

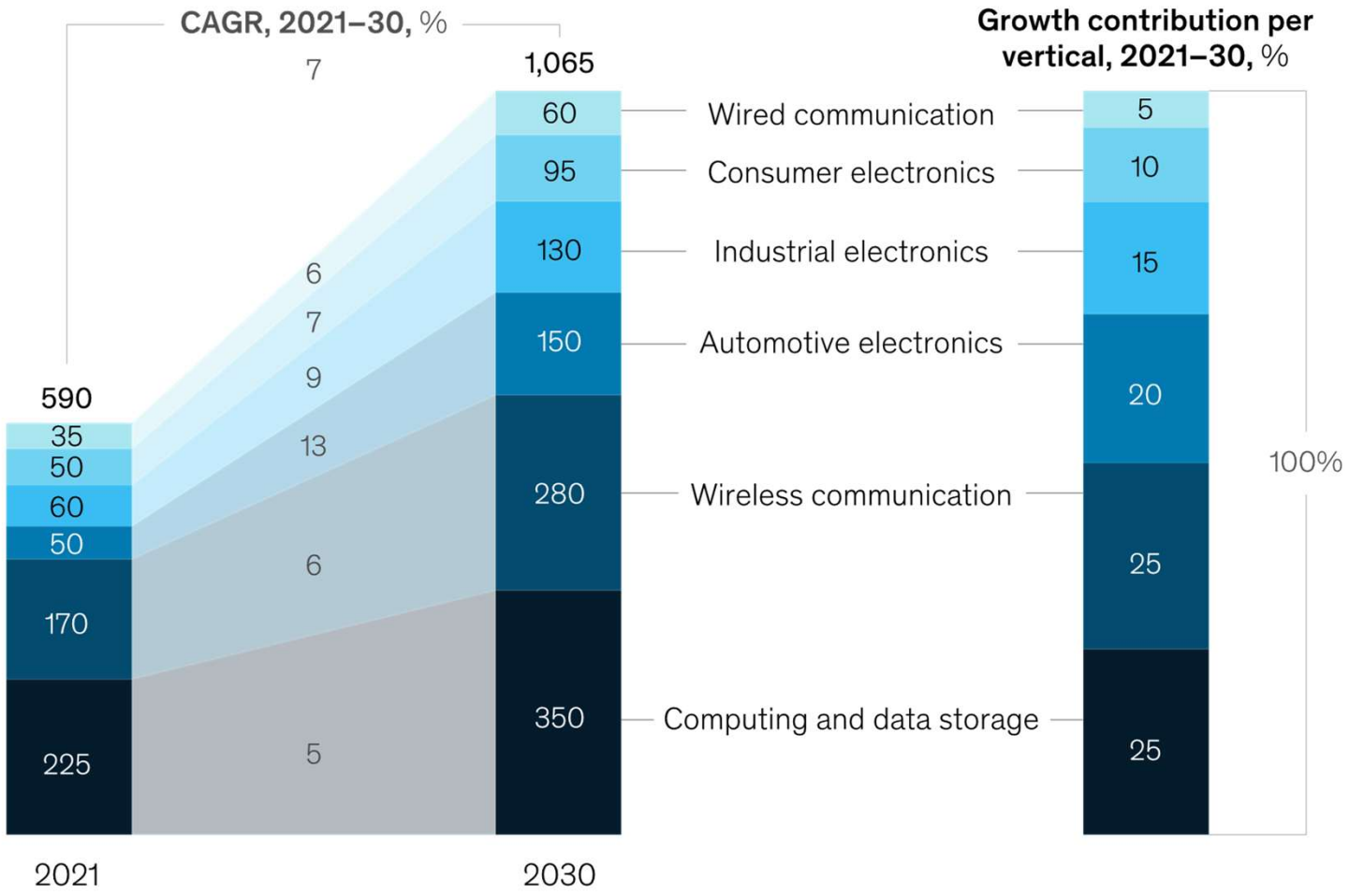
- Present in (literally almost) everyone's life
  - Arm case: >310B Arm based chips, 22M SW developers
- Changed humanity and how behaves
- Industry is globally strategic with strong geopolitical implications
- Topmost complex projects of engineering
  - One Chip Design in 3nm: $500M-$1.5B

Key Industry Growth Drivers

- AI & ML: Demand for accelerators (GPUs, TPUs).
- 5G and IoT: Connectivity explosion.
- EVs and ADAS: Automotive electronics boom.
- Cloud and Edge Computing: Server and device demand.

The overall growth in the global semiconductor market is driven by the automotive, data storage, and wireless industries.

Global semiconductor market value by vertical, indicative, $ billion

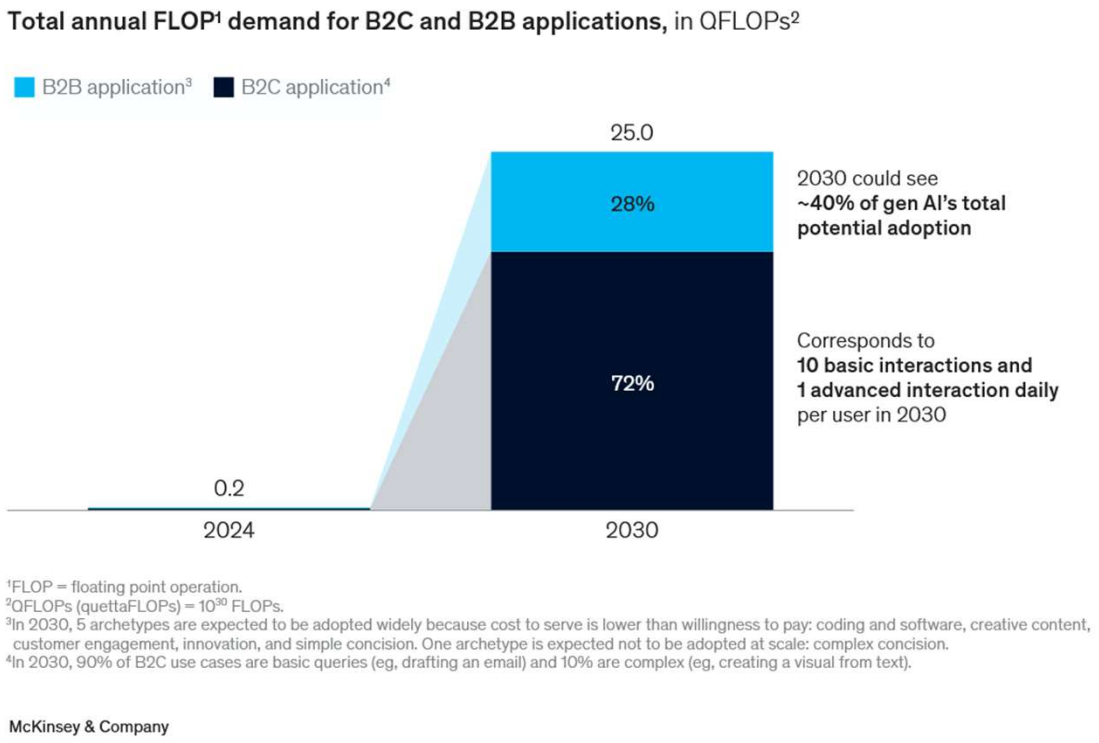


Note: Figures are approximate.

McKinsey & Company

Need for updated forecasts

- ChatGPT – 100M users in just two months (Instagram took 2.5 years)
    - 500M users in April 2025 (25% growth since February)



Source: Tap Twice Digital

The semiconductor industry

- Design: Front-end and Back-end engineering
- Manufacturing companies
- Test and validation companies
- Plus
  - Equipment
  - Material
  - Services

Semiconductor Design Houses

- Integrated Device Manufacturers

Fragmentation of the industry

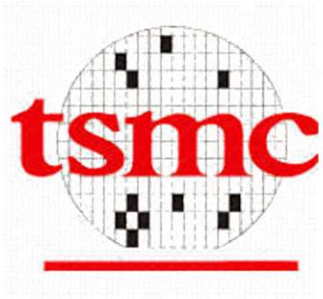
- Huge investments to keep-up

  → Gigantic investments need gigantic returns - scale

  →Focusing in one area with great expected outcomes

- Foundries (One fab line for 2nm - $20B - $30B)
  - IDMs do not have enough economies of scale

- A very large ecosystem



intel foundry

UMC

GlobalFoundries

Fabless companies

- Design-only firms that outsource manufacturing.
- Reduces CAPEX and increases focus on innovation.
- Heavy dependence on foundries like TSMC.

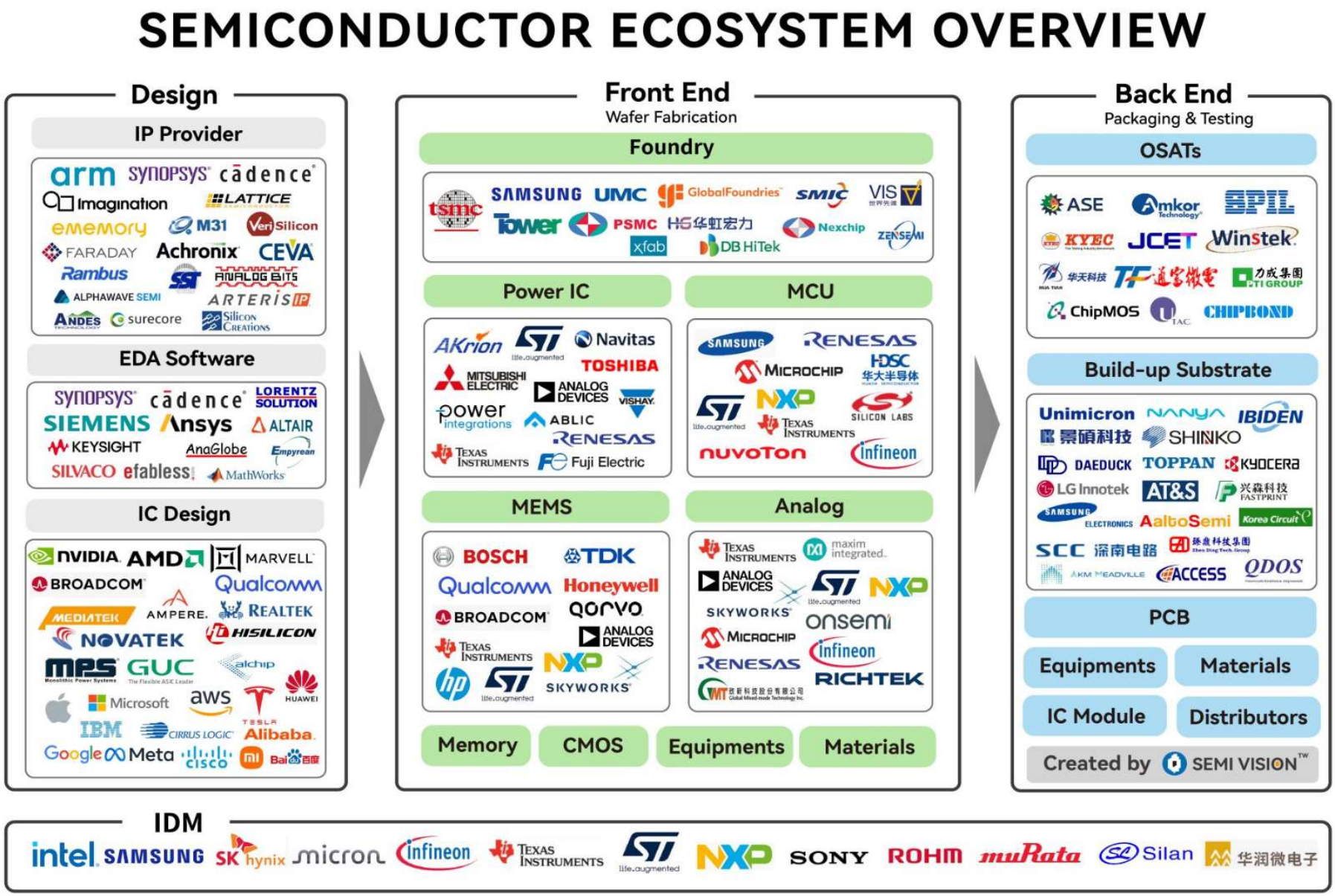
The Fabless

- IC Design Houses / Fabless

Semiconductor Value Chain

EDA/CAD & R&D/IP	Front-End & Back-End Design	Mask & Manufacturing (Fab)	Packaging/Test
cadence	Fabless	tsmc	Amkor Technology
SYNOPSYS	Design Services / Asic companies	SAMSUNG Foundry	UTAC
SIEMENS	GUC	intel foundry	
arm	SYNOPSYS		
Imagination	socionext		
Rambus	cadence		
	VeriSilicon		

A strongly interdependent ecosystem



Source: SemiVision

How can it work?

- Contracts, Patents, Law and Courts
  - Vs crushing power and physical security

How can it work?

- Contracts, Patents, Law and Courts
  - Vs crushing power and physical security
- Interdependence and the Prisoner’s Dilemma

How can it work?

- Contracts, Patents, Law and Courts
  - Vs crushing power and physical security

- Interdependence and the Prisoner's Dilemma

		Prisoner A	
		Collaborative - silent	**Opportunistic - betray**
Prisoner B	**Collaborative**	Each 1 month in jail	A free, B 1 year in jail
	Opportunistic	B free, A 1 year in jail	Each 3 months in jail

Semiconductor Industry Trends

The latest

- Shift towards fabless models for agility continues
- US-EU-Asia competition in chip sovereignty
- Rise of chiplets and heterogeneous integration
- M&A: Consolidation to control IP and capabilities

Semiconductor Industry Trends

Integrated Device Manufacturer (IDM)

- IDMs control the entire value chain from design to manufacturing
- High CAPEX but enables tight integration and performance tuning
- IDMs are resurging with geopolitical supply chain shifts.

Break

outline

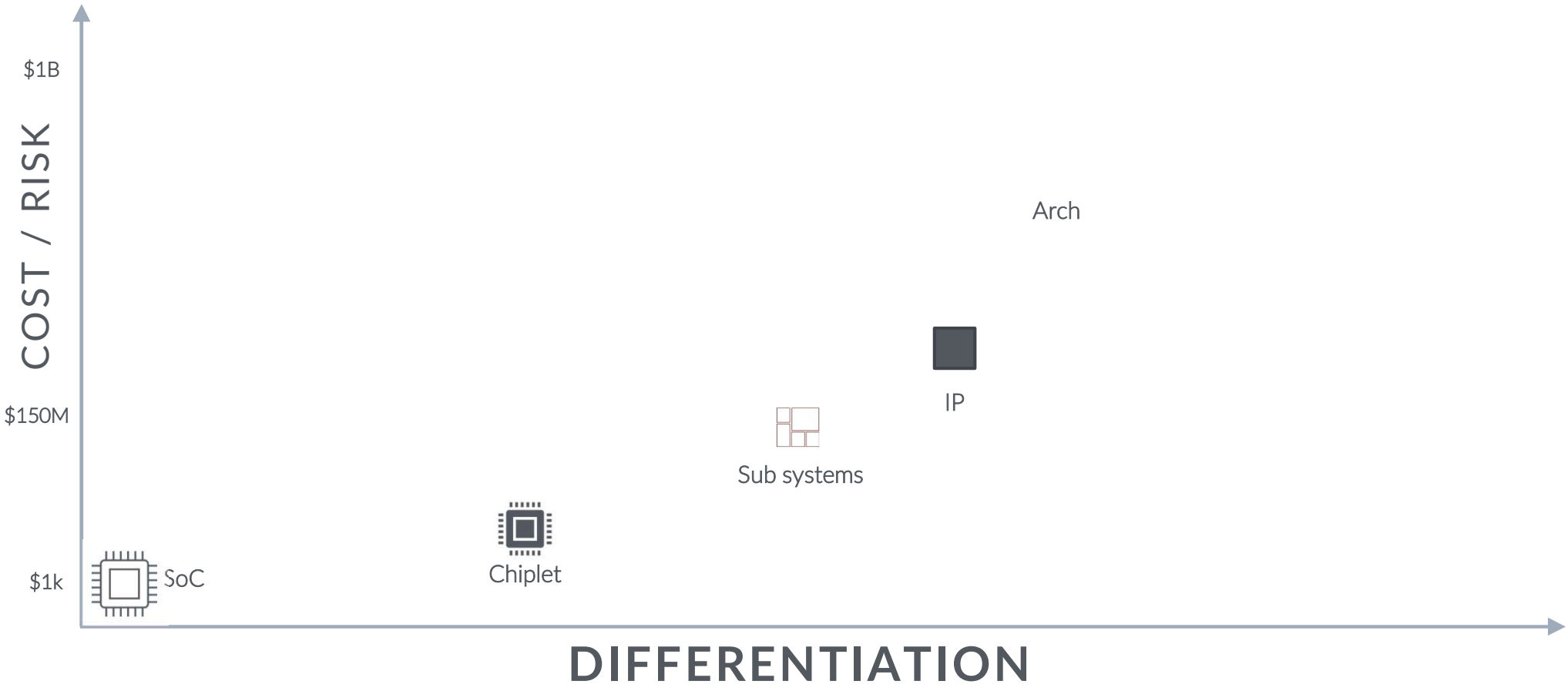
- 2 — the semiconductor industry — 27/06 — JMM
  - a — overview of the semiconductor value chain
  - b — value creation across the value chain
  - c — design-based business models
  - d — competitive opportunities

Semiconductor Value Chain

Development Costs per type of IC

Application	Node (Typical)	Chip Type	Chip Cost (USD M)	Software Cost (USD M)
AI/ML Accelerators	5nm / 3nm	High-end SoC	500-1500	100-300
Smartphones	5nm / 4nm / 3nm	Mobile SoC	250-500	50-150
Automotive (ADAS/ECU)	16nm / 28nm	Heterogeneous SoC	100-300	30-100
Networking	7nm – 28nm	DSP/SoC	100-250	20-70
Consumer Electronics	28nm – 40nm	Media SoC	50-150	10-40
IoT Devices	40nm – 90nm	MCU + Radio	10-30	2-10
Automotive (Legacy)	65nm – 180nm	MCU / ASIC	10-50	5-20
Industrial Automation	65nm – 130nm	MCU / SoC	15-40	5-15
Medical Devices	90nm – 180nm	Custom ASIC	25-100	10-30

Differentiation – the CPU case



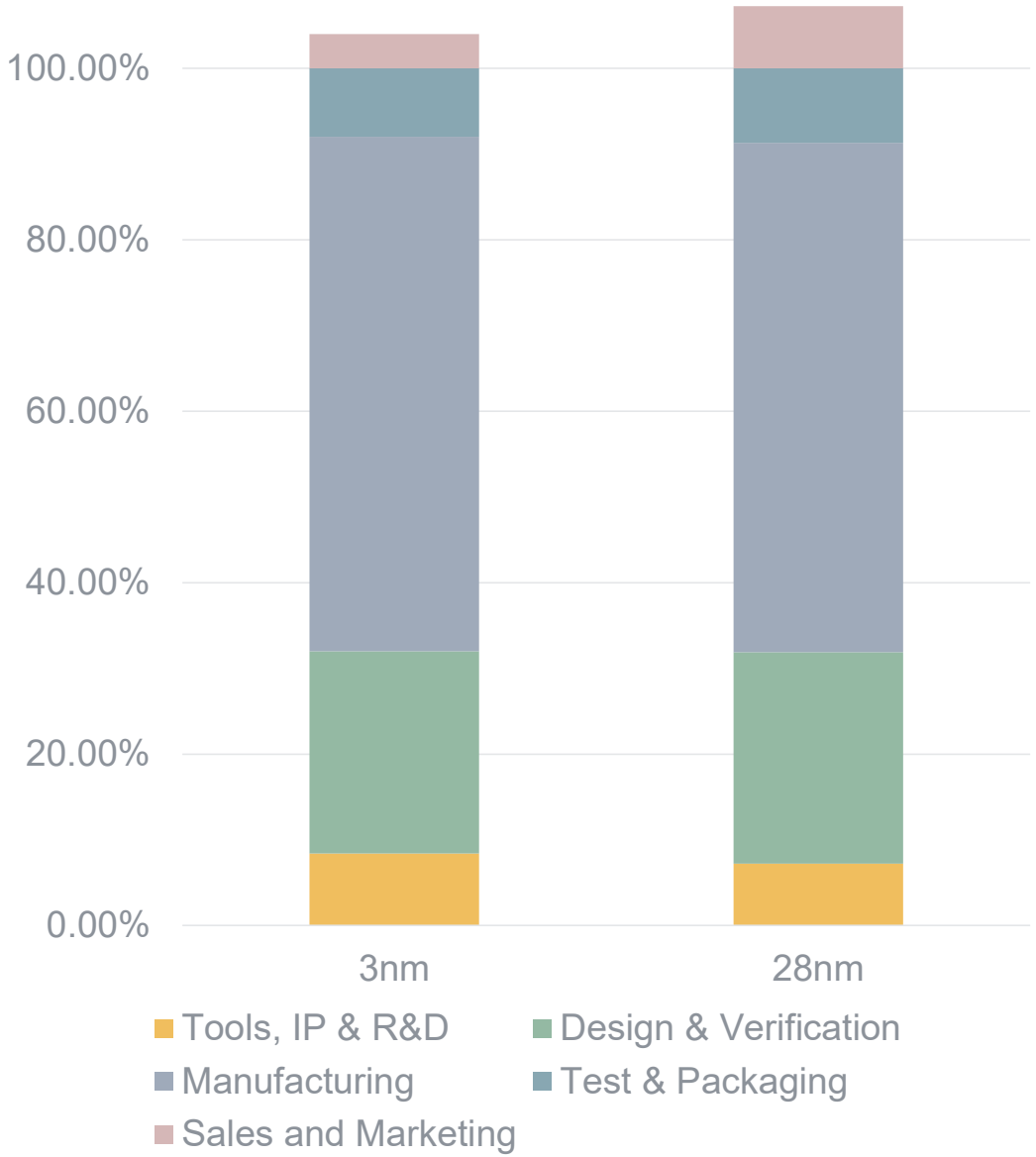
Semiconductor Value Chain

EDA/CAD & R&D/IP	Front-End & Back-End Design	Mask & Manufacturing (Fab)	Packaging/Test
cadence	Fabless	tsmc	Amkor Technology
SYNOPSYS	Design Services / Asic companies	SAMSUNG Foundry	UTAC
SIEMENS	GUC	intel foundry	
arm	SYNOPSYS		
Imagination	socionext		
Rambus	cadence		
	VeriSilicon		

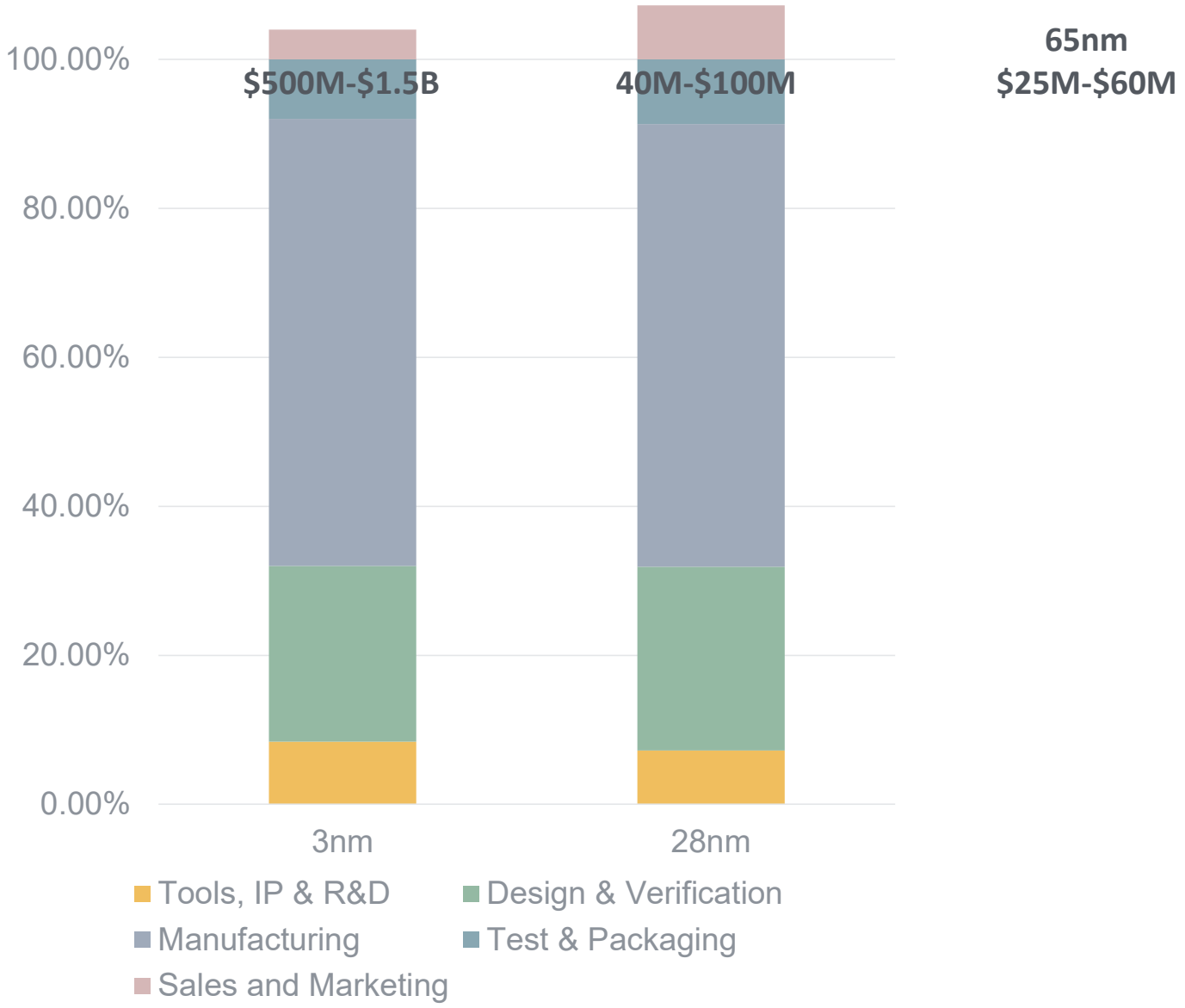
Cost of a chip

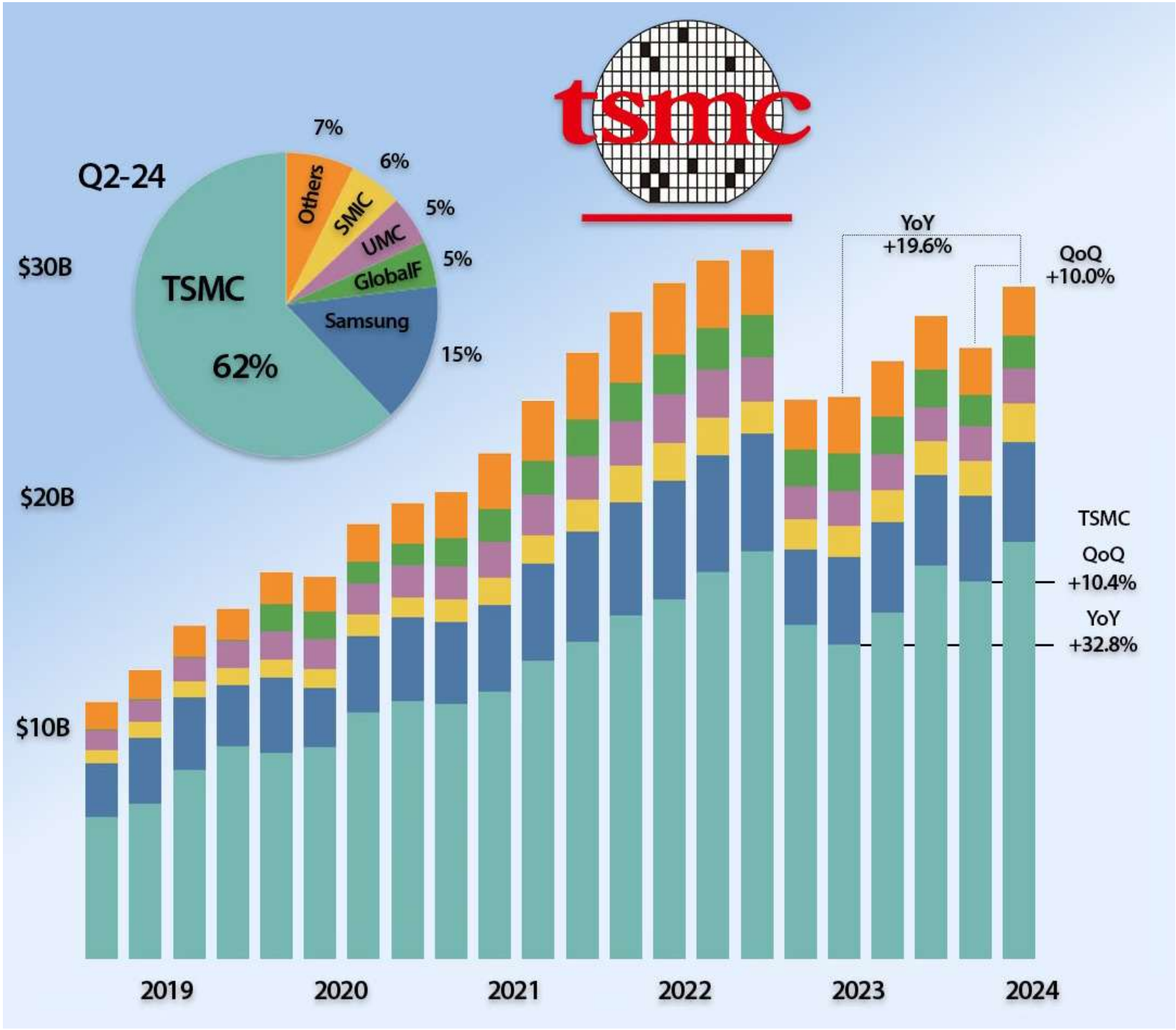
Marginal / volume based costs

Breakdown cost of a chip



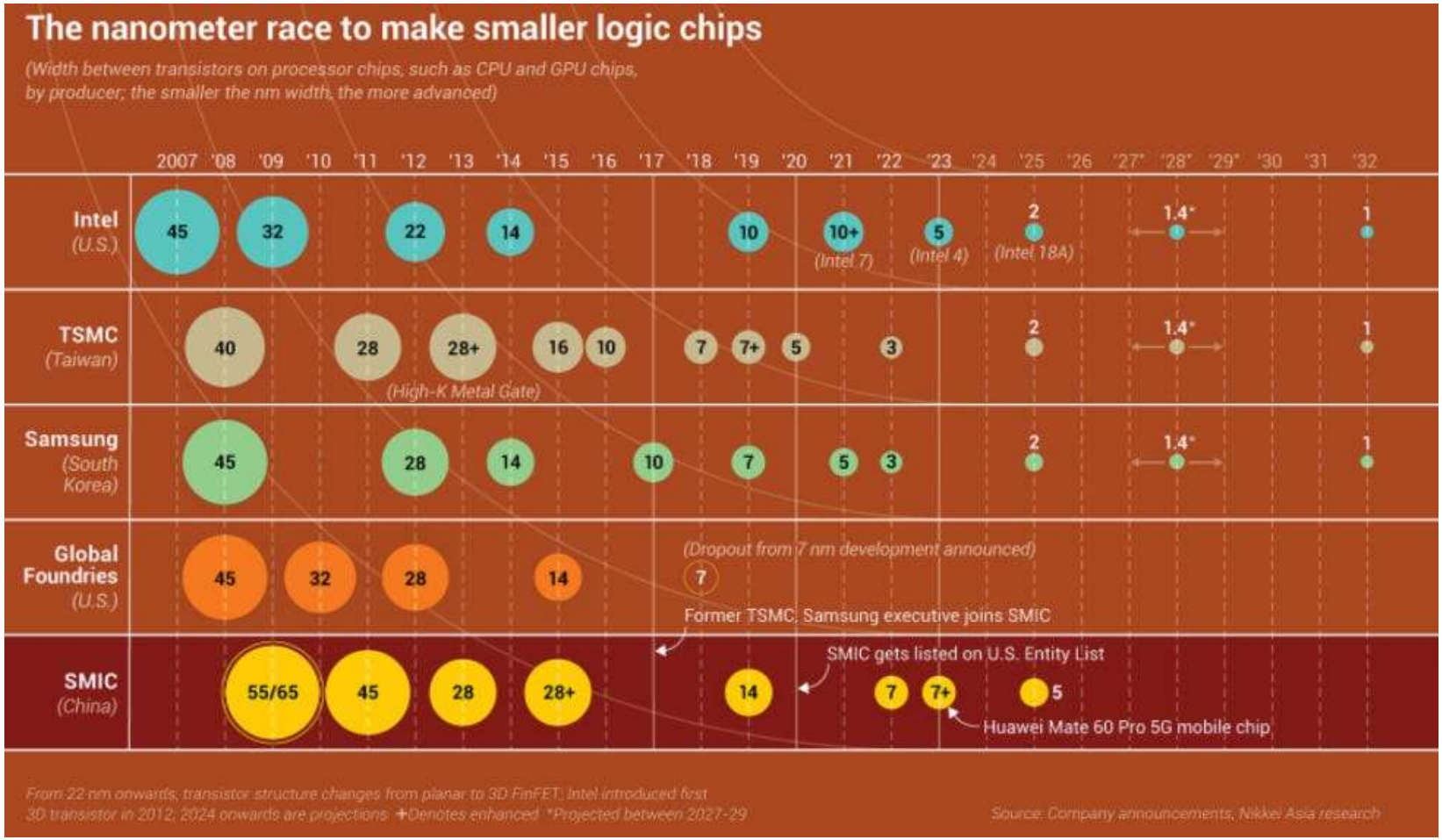
Breakdown cost of a chip

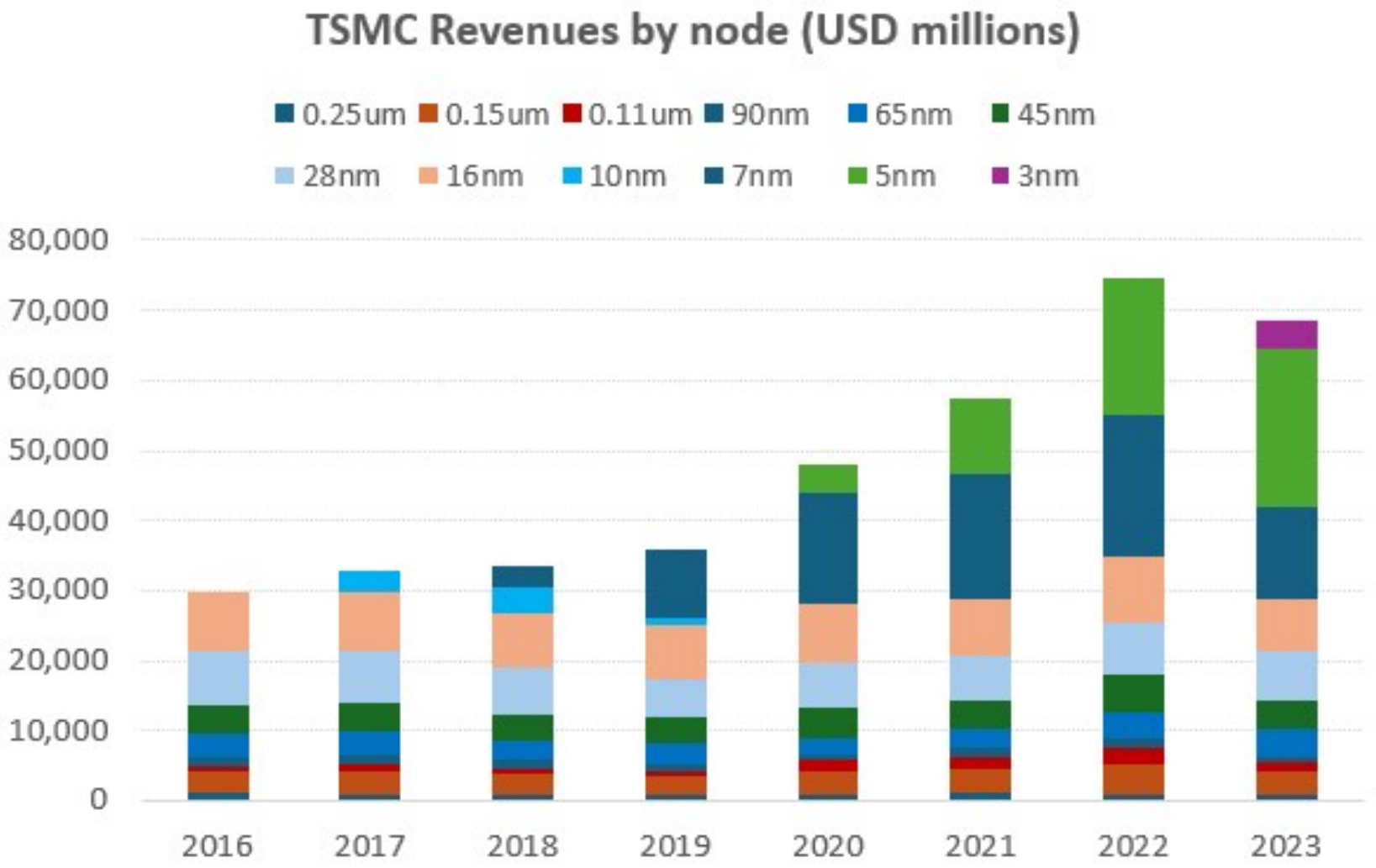




Source: SemiWiki

From 17 foundries @ 90nm





Source: Tech Investments

Semiconductor Value Chain

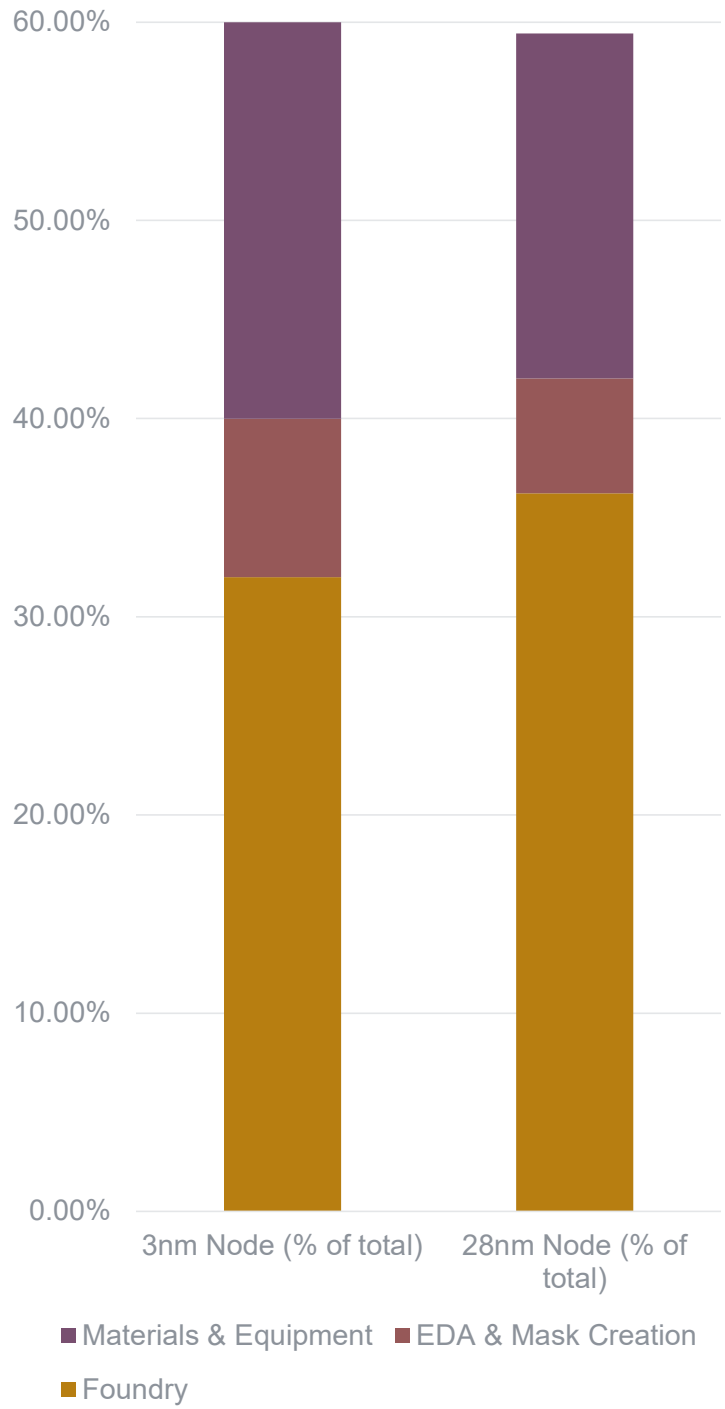
Mask & Manufacturing (Fab)

- Photomasks, or masks - define and transfer circuit patterns onto silicon wafers in photolithography process

- Manufacturing – wafers and high yield
  - Billions for a foundry
  - $20K for a 3nm wafer

Estimated total chip cost breakdown in leading edge and mature nodes:

- Capital equipment and materials (higher for leading-edge)
- Mask sets (more layers and reticle costs at smaller nodes)
- Cost of wafer fabrication



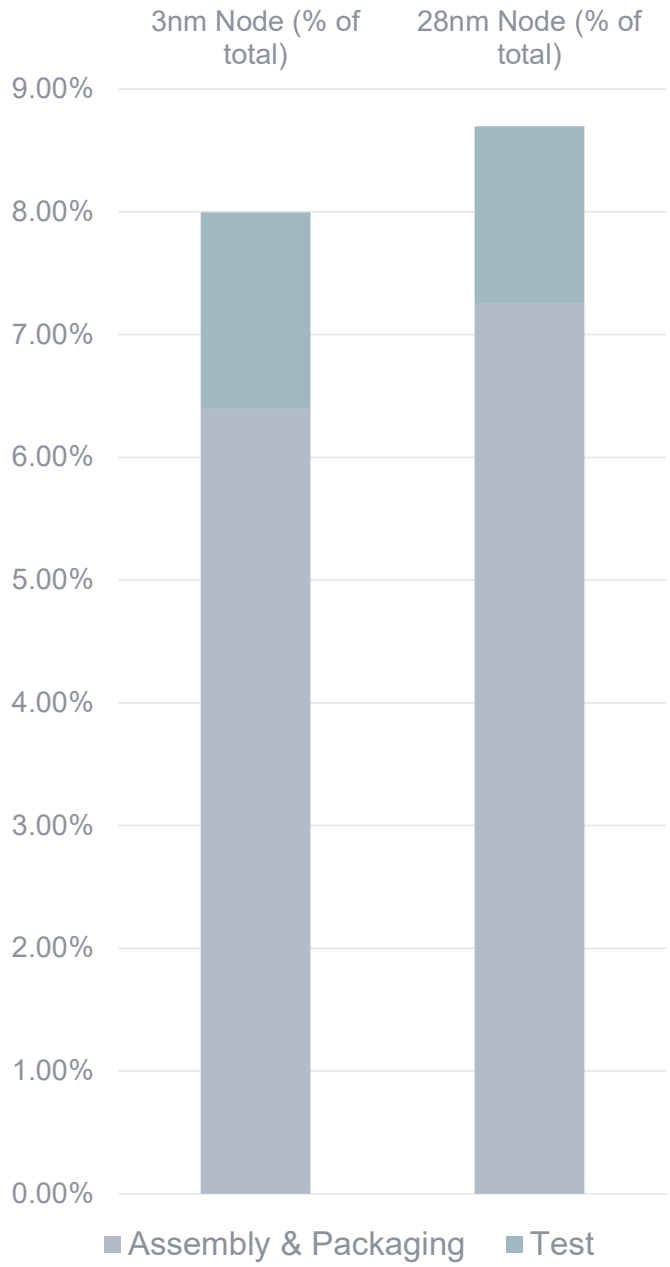
Semiconductor Value Chain

Packaging & Test

- Ensures performance, durability and reliability
- Packaging:
  - Protects
  - Electrical connections
  - Heat dissipation.
- Testing:
  - Verifies electrical, mechanical, and thermal performance criteria and reliability standards after packaging
  - Identify and discard defective chips

Estimated total chip cost breakdown in leading edge and mature nodes:

- Includes bumping, wire bonding, advanced packaging
- Electrical and parametric testing (more comprehensive at leading nodes)



Cost of a chip

Design costs

Semiconductor Value Chain

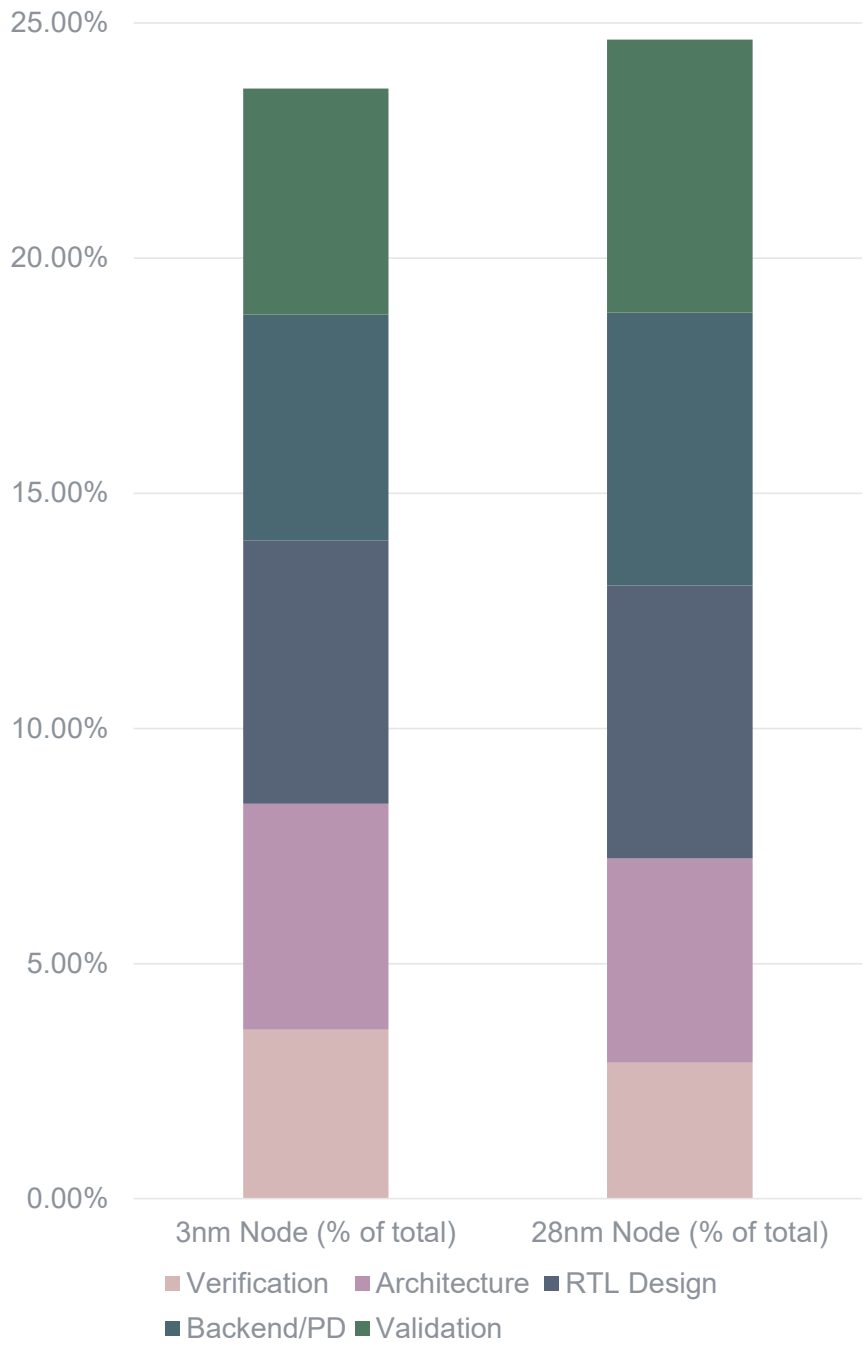
Front-end & Back-end Design

- back-end - physical implementation and manufacturing aspects
- front-end - logic and functional design of a chip

- Design is also an opportunity:
  - Outsourcing services
  - Licensing of IP

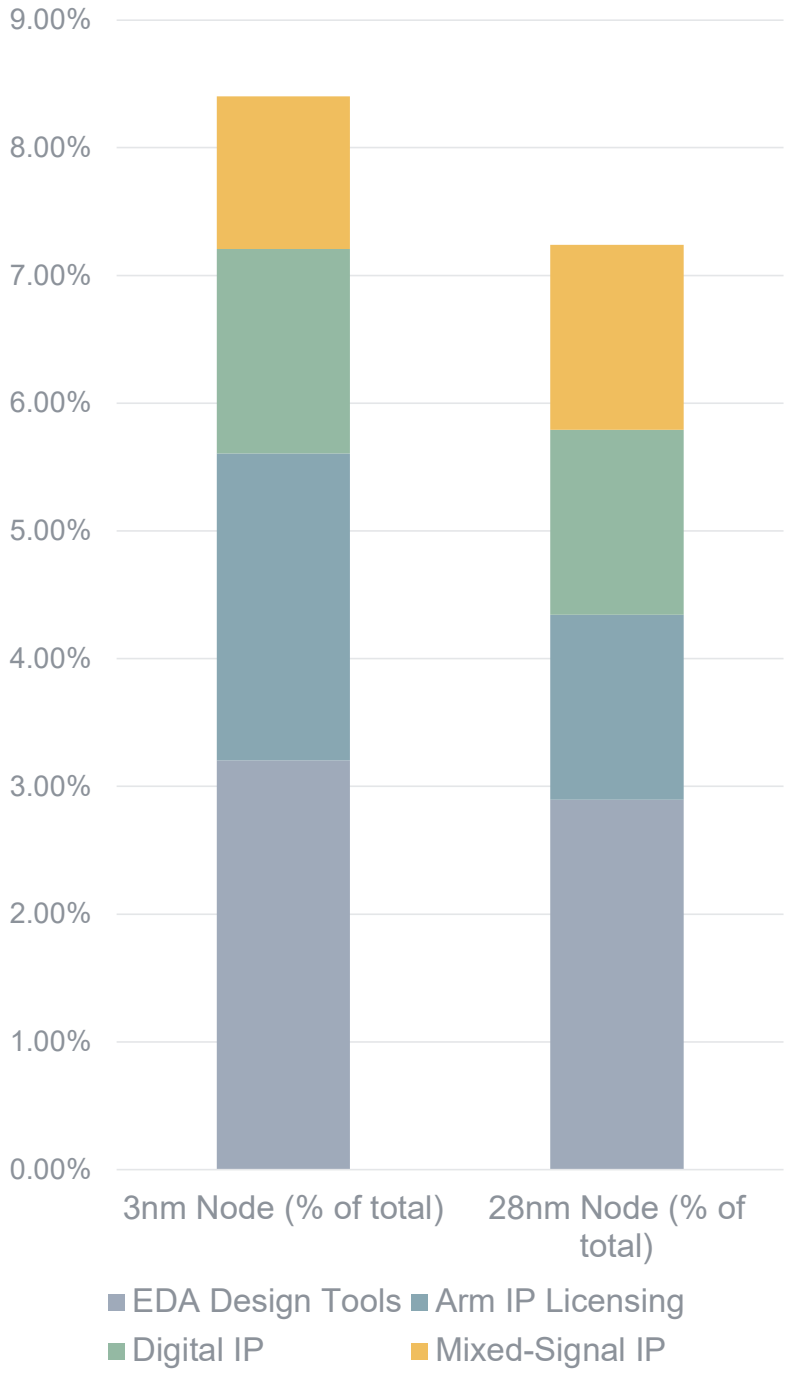
Estimated total chip cost breakdown in leading edge and mature nodes:

- Architecture
- Logic design
- Place & route, physical verification
- Post-silicon validation and functional testing
- Simulation, emulation, formal verification



Estimated total chip cost breakdown in leading edge and mature nodes:

- Tools
- Licensing cost for CPU/GPU
- Pre-verified IP blocks like interfaces, buses, etc.
- AMS cost covers both license and/or developed in-house



Semiconductor Value Chain

Electronic Design Automation (EDA) tools

- Schematic Design
- Design and Routing
- Simulation and Testing
- Design Verification
- Automation Efficiency

Semiconductor Value Chain

Intellectual Property (IP) - $7.5B in 2024 to $17.06B by 2034

- Processors CPU – arm, CAST, CEVA, IBM, MIPS, Synopsys, Cadence
- NPU – arm, Synopsys, Cadence, CEVA, Qualcomm
- GPU – arm, AMD, Imagination Technologies, Intel, NVidia
- Network-on-chip, Fabric – Arteris, arm, Cadence,Baya Systems,Intel:/Netspeed, AMD
- Physical IP – TSMC, Cadence, Synopsys
- Analog & Mixed-Signal - Analog Bits, Dolphin Semiconductor, Synopsys, Cadence, Silicon Gate, Arasan, Rambus,

Estimated total chip cost breakdown in leading edge and mature nodes:

- Tools
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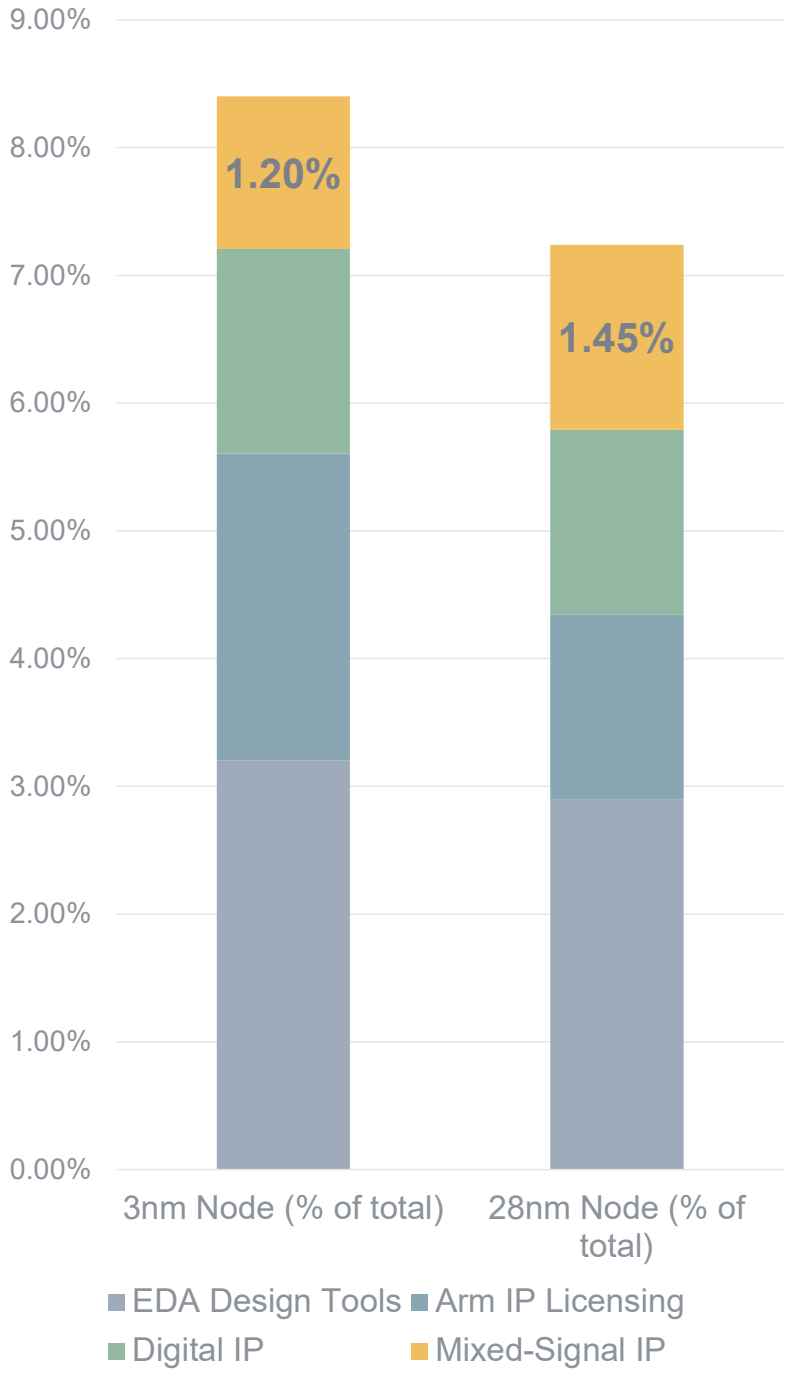

Semiconductor Value Chain

Analog Mixed-Signal IP

- AMS in a Design:
  - 3nm: $6M-18M
  - 28nm: $.5M-1.2M
- RF (5G, IOT), Power Management (Auto), Data Converters (Auto, Telco) and High-Speed Interfaces
  - WW CAGR of 15.17% from 2025 to 2030

Break

outline

2 the semiconductor industry 27/06 JMM

- a overview of the semiconductor value chain
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- d competitive opportunities for europe

Design-Based Business Models

Fabless Chip Companies	Design Services	IP Companies
Specs Ownership Silicon Delivery	Customer Ownership of Specs Silicon or Data Transfer Delivery as works for hire	Specs Ownership Data Transfer with rights to use

Fabless Chip Companies

- Focus on IC design; outsource manufacturing to foundries
  - Define specifications and architecture
  - Logic design and RTL coding
  - Verification and physical design
  - Manufacturing, testing, and iteration.
- Advantages: Will get a higher value, but needs to address higher costs (vs IP or Design Services)
- Challenges: Investment, supply chain risk, dependence on many suppliers, including foundries, and **having the right product**

Fabless Chip Costs

- Personnel costs – engineering talent (design, verification, architects, layout, management, sales and marketing, lawyers)
  - The usage of third party services is highly recommended
  - Depending on the system, may need massive investment in software

- EDA Software licenses
- Technology / IP licensing
- Fabrication costs
- Testing and Packaging
- Legal and regulatory costs (patents, compliance export controls etc)
- Operations
- Sales, Marketing, and Distribution
- Logistics and Inventory Management
- etc

Fabless Chip Revenues

- Chip Sales directly – needs volume and margin
  - Reference Designs / Samples

- Distribution of chips via channels or OEMs or system integrators
- Licensing of Technology (Fees + Royalties)
- Non-Recurring Engineering (NRE) Fees for customization
- Partnerships / Joint Ventures payments
- Supporting Software and Tools
- Sale of assets

Design Services & Custom Solutions

- Custom design services (silicon, front end design, backend etc) on behalf of a customer
- Synopsys, Cadence, AMD, CapGemini, GUC, Alchip, Socionext, Wipro, VeriSilicon, Mediatek, Faraday etc
- Advantages: Less upfront investment, more reactive, no need to foresee a roadmap, but can protect technology with “background IP”
- Challenges: Limited scalability, project-based revenue, highly competitive / lower margins unless you have unique know-how / technology

Design Services Costs

- Personnel costs – engineering talent (design, verification, layout, technical leads, management, sales and marketing)
  - Increased Project Management integrated with the customer
- EDA Software licenses
- Infrastructure and IT
- IP acquisition and licensing costs
- Operations
- Training and development
- Legal and regulatory costs (patents, compliance export controls etc)
- Sales, Marketing
- etc

Design Services Revenues

- Engineering Service Fees for silicon, IP, software etc (Man-hour, M-H packages)
- NRE, mainly for customization
- Turnkey ASIC Design Services
  - ASIC production services
- Licensing technology
- Support, maintenance, training and advisory

IP Companies

- Develop a core technology with reusable IP blocks and a roadmap (e.g., CPU cores)
  - Soft IP (RTL) vs Hard IP (GDSII layout).
- Advantages: Scalable revenue, high margins, low operational cost, critical for fast, low-risk SoC/ASIC development.
- Challenges: Requires ongoing innovation, strong competition, stickiness of the technology

IP Companies Costs

- Personnel costs – engineering talent (design, verification, architects, management, sales and marketing, lawyers)
- Increased Customer Support & Integration
  - FAEs, documentation, sometimes customization
- Software Development
  - SDKs, drivers, integration tools
- EDA Software licenses
- Infrastructure and IT
- IP validation and Test Chips
- Standards, Certification, Interoperability
- Legal and regulatory costs (patents, compliance export controls etc)
- Sales & Marketing~~, and Distribution~~
- etc

IP Companies Revenues

- License Fees (Upfront and recurrent)
  - One-time payments for IP rights
  - Subscription for portfolio access
- Royalties (Per Unit shipped by customer)
- Support and Maintenance
- Training
- Fees for customization / porting
- Partnerships / Joint Ventures payments
- Supporting Software and Tools
- Sale of assets

Licensing

Licensing

"A slice, not the full cake" – **if not stated, right does not exist**

Licensing

Silicon /OEM companies

- Evaluate or Limited Use Licenses (not an NDA)
- Design
  - Sharing with EDA
  - Subcontracting rights
- Manufacturing & Testing
  - Have Manufacturing rights
  - Have Testing rights

Licensing

Design and tape out – variations with different fees

- Single Use
  - Bundle of Single Uses
  - Derivatives
  - Time limited
- Term Use
- Perpetual Use
- Subscription

Licensing

Royalties

- Royalties are hard to get
- Stickiness is key
- Patents or ecosystem is the way to get royalties but it is hard to achieve such position
- Insight bias and cost to opt out

Licensing

EDA or Other IP Companies

- EDA Debug rights
- Tools improvement
- Scripts
- Benchmarking
- Marketing
- Interoperability

Licensing

Foundries

- Benchmarking by a foundry
  - Benchmark
  - Improve process
  - Tools debug and improvement
  - Scripts debug and improvement
  - Marketing
- Foundry Model – porting fees

Disclaimer
I am not a lawyer
This is not legal advice

Licensing

Other issues with Licensing

- Warranty ONLY for i) Infringement and ii) Fitness for a purpose
  - Functional for substantial conform with specs
  - No coverage due to implementation
  - Subject to active maintenance (updated IP in the SOC)
- Liability – ONLY for the warranty, and NOT responsible for any other costs, direct or indirect
  - Negligence and fraud is always a liability

Licensing

Other issues with Licensing

- Liability / Indemnity cap
  - IP infringement (one or two ways?)
  - Personal Liability for Negligence and Fraud not limited
  - Cap to amounts paid – % of total NRE, Fees, sometimes Royalties and and S&M

Licensing

Other issues with Licensing

- Technology protections:
  - Patents vs. common law Copyrights / Trade Secrets
- Exclusivity:
  - To avoid
  - If not, strongly limit – what, how is implemented, where, when, markets, products etc

Break

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Where is the Opportunity?

Analog & Mixed Signal

- Rapid growth in IoT, automotive, and healthcare sectors
- Increasing demand for high-quality analog IP (ADC/DAC, PLL, power management)
- Connectivity IP allows easier reuse: PCIe, MIPI, etc, and for chiplets, UCIe etc…
- High profitability through differentiated analog/mixed-signal IP
- Strong opportunity for startups and niche fabless companies

Where is the Opportunity?

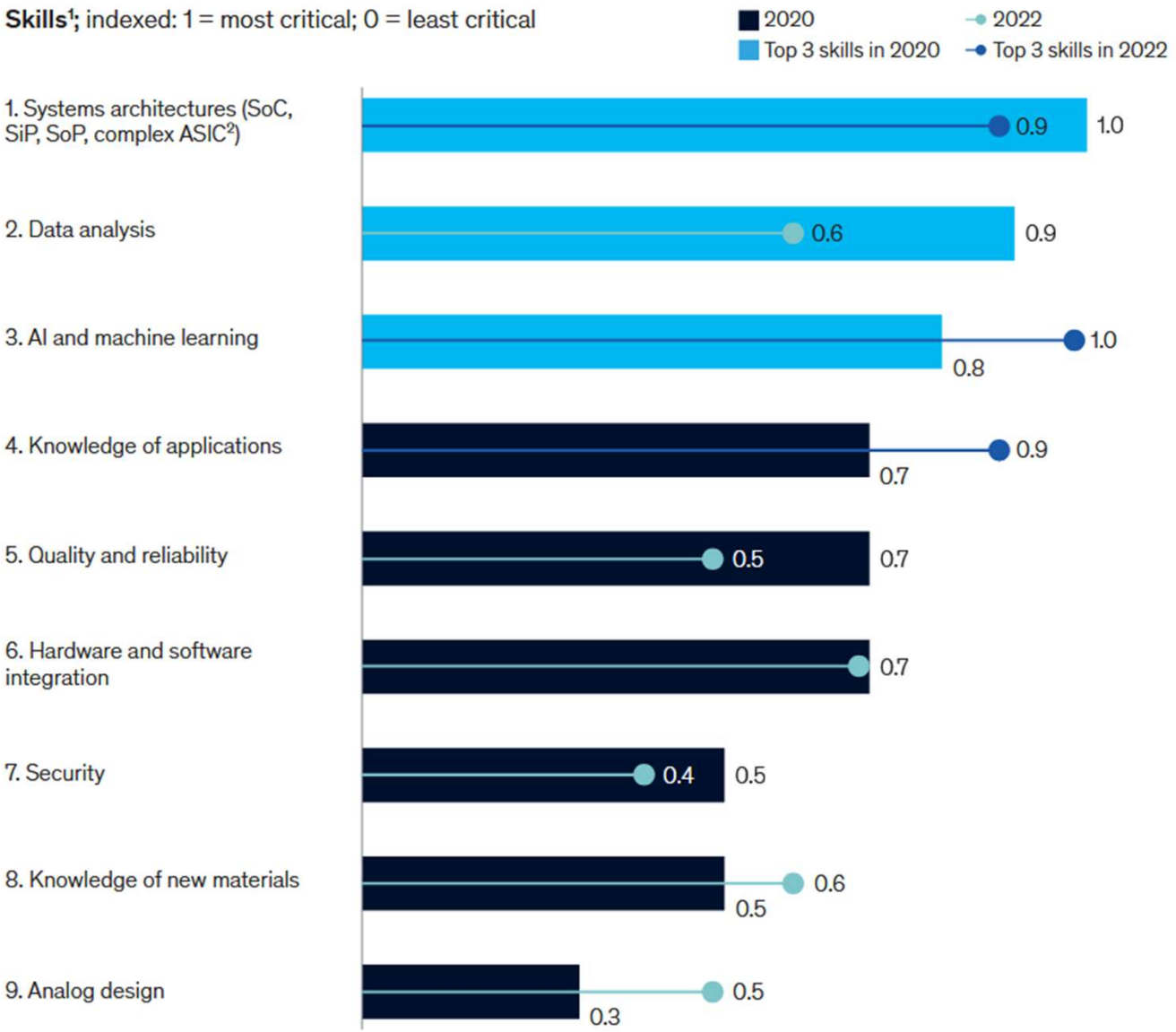
Problems to be solved.

- Is there a practical problem to solve that everyone got used to?
- Address a real need, or products that would make a real difference (a product can be a technological solution dully packaged and usable)
- Differentiate - stay away from price competition
- Stay away of developing “a great technological solution” – solve a problem instead.

A possible chart

- Find a profitable problem to solve or need to address, but with a purpose
- Find good people to work with
- Try to be independent (do not count on subsidies etc)
- Be flexible and in phases, expect the worst, plan for the best
- It is ok to not know it all - trust yourself and that it is ok to fail
- Believe that if change is dangerous, that routine is lethal – “magic” happens out of your comfort zone

AI and machine-learning skills have recently replaced system architecture knowledge on the European job market.



[1]The skills most sought-after by companies and those most difficult to find on the European job market.
[2]System-on-a-chip, system in package, system on package, application-specific integrated circuit.
Source: Léo Saint-Martin, *METIS skills strategy*, SEMI, November 18, 2021; *Yearly monitoring report 2022*, SEMI, 2022; McKinsey analysis

McKinsey & Company

EMBRACE FAILURE

Open discussion