Seasonal School on Advanced Analog and Mixed-Signal (AMS) IC Design 2025

Powered by POEMS - Microelectronics Academy

June 12 - July 31

7 weeks
9h30 – 17h30

Technical Sponsors:

Semiconductor Entrepreneurship

Purpose

The purpose of this semiconductor entrepreneurship course is to equip students with the knowledge and skills to identify, develop, and commercialize innovative technologies in the semiconductor industry, while fostering the creation of semiconductor startups.

1997

3 people

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Leading EU Talent Hub

2000 people

6 major multinationals

20 global startups

2035

The world will notice it!

The Startup Journey in the Semiconductor Industry

From Problem Discovery to Fundraising in B2B Startups

José E Franca

Start2Scale | IST

remember your 6-week project

NewCo Idea

This is the a-to-z startup journey

1. what is the problem/need you are solving
2. who might be interested in the problem
3. how do you propose to solve it
4. who else has a solution for the problem
5. how competitive is your solution
6. can you sustain your solution
7. how do you make money
8. what do you need to make that money
9. what could be your 5-year financial projections (accounts management viewpoint)
10. with who are you going to do all that (existing, hiring, advising)

This is what we will cover today

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Agenda

- What can you do with your AMS design talent?
- Why Semiconductor Startups Are Unique
- Problem Discovery in Semiconductor B2B Context
- Investor Perspective on Deep-Tech Problems
- Solution Development in Semiconductors
- Competitive Positioning in the Ecosystem
- Case Studies & Interactive Exercises

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What Can AMS Design Engineers Do With Their Talent?

Build the Foundations of Tomorrow's Tech

Analog and mixed-signal engineers are essential to:

- Sensor interfaces in wearables and medical devices
- Power management in AI accelerators and automotive chips
- High-speed data converters for 5G/6G and edge computing
- RF front-ends for connectivity and radar
- Sensing in autonomous driving

You don't just design circuits.
You build the bridges between the analog world and the digital world.

What Can AMS Design Engineers Do With Their Talent?

Drive Innovation from the Ground Up

AMS designers often:

- Push Moore’s Law forward when digital scaling hits limits
- Enable chiplet integration, 3D ICs, and advanced packaging
- Solve real-world problems — from signal integrity to energy efficiency

Most breakthrough systems — from pacemakers to LiDAR rely on a robust AMS core.

What Can AMS Design Engineers Do With Their Talent?

Launch Deep-Tech Startups

Your skillset enables:

- Creating IP blocks (e.g., ADCs, PLLs, SerDes) for licensing or platform play
- Designing application-specific ICs (ASICs) for verticals like medical, aerospace, or mobility
- Developing EDA tools or AI-assisted design platforms
- Innovating in chip security, noise resilience, or low-power design

Chipidea, Acacia, SiliconGate, Power Tools, and many others, all started with engineers like you identifying a hard problem and solving it better than anyone else.

What Can AMS Design Engineers Do With Their Talent?

Lead in the Next Frontier of Entrepreneurship

AMS engineers are uniquely positioned to:

- ✦ Found or join hardware startups with real IP
- ✦ Be technical founders that VCs value for their credibility
- ✦ Collaborate with system architects to build next-gen products
- ✦ Become CTOs, IP architects, or innovation leaders

Investors are now chasing differentiated, hardware-centric ideas — and you speak the language of physical reality.

What Can AMS Design Engineers Do With Their Talent?

Shape a Better World with Precision and Power

- ✦ Healthcare: Medtech, Implantable chips, biosignal acquisition, neuromodulation
- ✦ Energy: Smart grids, high-efficiency power converters, battery management
- ✦ Mobility: Radar, lidar, EV chargers, motor control
- ✦ Environment: Precision sensing for pollution, agriculture, or climate tech

In a noisy, fast world — AMS engineers deliver clarity, precision, and power efficiency.

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Why Semiconductor Startups are Unique

Deep Tech Complexity

- **High technical barrier to entry**: Startups often need deep expertise in device physics, circuit design, packaging, and process technology.
- **Long development cycles:** It can take 12–36 months to go from idea to a working silicon prototype.
- **System-level thinking**: Success often depends on tight integration of hardware, software, and application context.

“You’re not just building a product, you’re engineering physics into solutions.”

Why Semiconductor Startups are Unique

Capital Intensity

- Salaries of highly qualified engineers
- Tool licenses (EDA), MPW shuttle runs, lab equipment are expensive.
- Even a basic tape-out (e.g., on a mature 180nm node) costs **tens to hundreds of thousands of euros**.
- Series A/B rounds for semiconductor startups often require **€10M+** to reach product-market fit.

This isn’t code you can launch from your laptop. Capital planning and investor selection matter.

Why Semiconductor Startups are Unique

Ecosystem Dependence

- Startups must plug into a complex supply chain: foundries, IP vendors, packaging houses, tool providers, lab equipment vendors.
- Design wins depend on **interoperability** with Cadence, Synopsys, Siemens, ARM, TSMC, etc.
- **Pre-qualification** and **platform compatibility** are often critical for customer adoption.

“A chip doesn’t live alone — it’s part of a web of standards, dependencies, and integrations.”

Why Semiconductor Startups are Unique

Long Sales Cycles

- In B2B semiconductors, sales cycles can last **6–24 months** — due to evaluations, PoCs, and design integration.
- Stakeholders include engineering teams, CTOs, procurement, compliance, and of course the CEO.

Founders must be patient and technically credible — shortcuts don’t work in this space.

Why Semiconductor Startups are Unique

High Trust & Validation Requirements

- Customers want silicon-proven IP, reliability, foundry compatibility, and standards compliance.
- New startups must often secure **anchor customers**, joint development agreements, or silicon validation.

In this business, “fake it till you make it” is not an option.

Why Semiconductor Startups are Unique

Barriers to Entry Are Also Moats

- Once a startup breaks through with a verified, adopted solution (e.g., IP block, EDA tool, or ASIC service), the **barriers that made it hard to start** become **defensible moats**.
- Customers don’t switch silicon vendors or design tools easily.

“High friction in = high defensibility out.”

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Problem Discovery in Semiconductor B2B Context

Understand the Nature of Problems in Semiconductors

- Problems are rarely visible at the surface — they often lie deep within **design flows**, **toolchain gaps**, **yield issues**, or **integration pain points**.
- Many pain points persist due to legacy tools, high switching costs, or lack of bandwidth in engineering teams.

“In semiconductors, engineers often don’t have time to fix what’s broken — that’s where startups step in.”

Problem Discovery in Semiconductor B2B Context

Where to Look for Real Problems

A. Design & Verification Workflows

- Slow simulation times, complex analog–digital co-design, poor test coverage, versioning nightmares.

B. IP Reuse and Integration

- Reuse is promised but rarely smooth; integration across process nodes or toolchains is often messy.

C. Manufacturing & Packaging Bottlenecks

- Chiplet integration, thermal issues, or design for testability constraints.

Every step in the chip journey — from RTL to GDSII to silicon — hides dozens of unsolved problems.

Problem Discovery in Semiconductor B2B Context

Where to Look for Real Problems

D. Supply Chain & Yield Management

- Poor visibility across stages, lack of tooling for yield optimization, or weak failure diagnostics.

E. Cross-Domain Transitions

- Hardware/software co-design, sensor-fusion calibration, power management in high-density designs.

Every step in the chip journey — from RTL to GDSII to silicon — hides dozens of unsolved problems.

Problem Discovery in Semiconductor B2B Context

How to Uncover These Problems

A. Interviews

- Talk to design engineers, verification leads, test engineers, and foundry liaisons.
- Ask: “What slows you down the most?”, “What would you automate if you could?”

B. Shadow the Workflow

- Observe how teams handle design handoff, IP integration, DRC fixes, or debug cycles.

C. Failure and Post-Mortem Reports

- Many design issues only surface after first silicon — read technical conference papers, customer debriefs, or teardown reports.

D. Gap Analysis

- Compare the capabilities of leading EDA or IP vendors with new emerging needs (e.g., chiplets, ML-assisted design).

Problem Discovery in Semiconductor B2B Context

Criteria to Prioritize the Problem

- **Severity**: Is it slowing down teams significantly?
- **Frequency**: Does it affect every design, or just niche use cases?
- **Budget Ownership**: Is someone in the org responsible and willing to pay to fix it?
- **Strategic Value**: Would solving it lead to broader platform opportunities?

A good problem is one that is urgent, costly, frequent, and currently underserved.

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Investor Perspective on Semiconductor Problems

Severity & Pain Level

- Is the problem painful enough that customers are actively seeking (and paying for) solutions?
- Is it causing loss of time, money, productivity, or compliance risk?

“Nice-to-have” problems rarely get funded.
Investors want “hair-on-fire” problems.

Investor Perspective on Semiconductor Problems

Frequency & Ubiquity

- How often does the problem occur in the customer's workflow or operations?
- Is it a daily pain or an occasional inconvenience?
- How widespread is the problem across a market or vertical?

Investor Perspective on Semiconductor Problems

Economic Value of Solving it

- Can the solution drive revenue growth, cost reduction, risk mitigation, or regulatory compliance?
- Is there a clear ROI case (e.g., “Save $1M/year in tape-out errors”)?
- Does the problem link to key performance indicators (KPIs) at the enterprise level?

Investor Perspective on Semiconductor Problems

Urgency & Timing

- Is this problem becoming more urgent due to external shifts (e.g., regulation, supply chain disruptions, new technologies)?
- Does it align with macro trends like AI, chiplet architectures, automotive safety, or energy efficiency?

Investor Perspective on Semiconductor Problems

Willingness to Pay & Budget Ownership

- Do target customers have budget authority and willingness to pay for a solution?
- Is there an existing budget line item or does it require creating a new one (which can be a hurdle)?
- Who in the company owns the pain and the purse strings?

Investor Perspective on Semiconductor Problems

Market Size

- How big is the Total Addressable Market (TAM) associated with the problem?
- Can solving it lead to a venture-scale opportunity (typically >$1B TAM)?
- Are there adjacent markets once the initial segment is won?

Investor Perspective on Semiconductor Problems

Barriers to Solution / Entrenchment of the Problem

- Are current solutions inadequate or outdated?
- Is there a clear gap or friction that can’t be addressed by incumbents due to legacy issues or misaligned incentives?

Investor Perspective on Semiconductor Problems

Strategic Leverage

- Can solving this problem lead to a platform opportunity, enabling further value capture (e.g., becoming the de facto tool in a flow)?
- Could it open doors to high-value partnerships or long-term vendor lock-in?

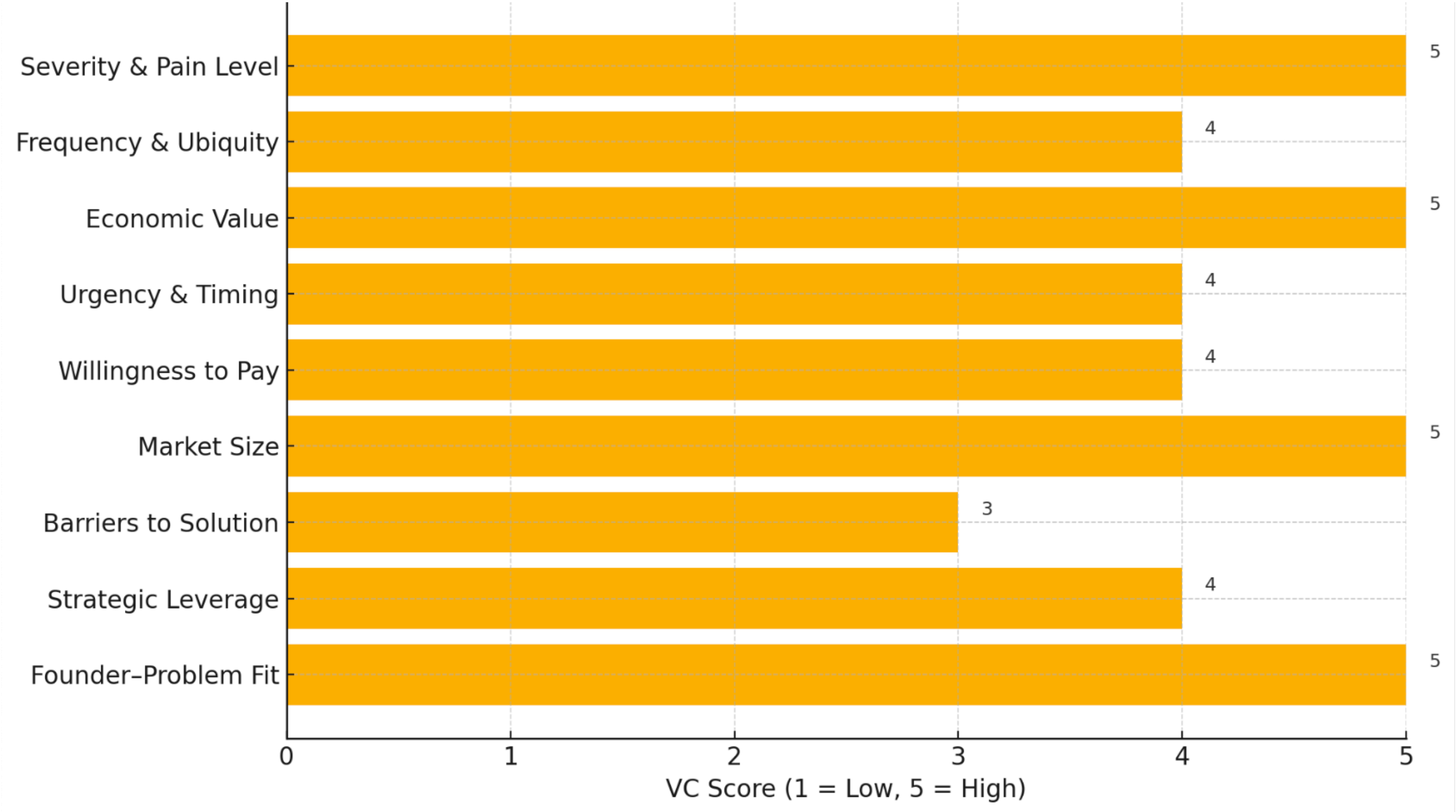
Investor Perspective on Semiconductor Problems

Founder–Problem Fit

- Does the founding team have unique insight, experience, or access that makes them especially qualified to solve this problem?
- Many investors say, “I invest in problems, not products.”
- A compelling, painful, and valuable problem is the bedrock of a fundable startup.

Investor Perspective on Semiconductor Problems

How Investors Score the Attractiveness of a Startup Problem



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Solution Development in Semiconductors

Why It’s Different

- Customers (e.g., chip design teams, system integrators, foundries) have zero tolerance for half-baked or flaky solutions.
- Solutions must meet performance, area, power, reliability, and compatibility specs — often simultaneously.
- Hardware, IP, and EDA solutions are deeply embedded into mission-critical workflows — switching is hard and trust is everything.

“In semiconductors, your MVP must already behave like a version 2 product — because customers can't afford to gamble.”

Solution Development in Semiconductors

Solution Types

Depending on the startup's nature, the solution might be:

A. Semiconductor IP

- E.g., ADCs, PLLs, SerDes, AI accelerators
- Must be delivered as RTL or GDSII, with verification suites, datasheets, PPA metrics, and possibly silicon validation

B. EDA Tools or Plugins

- Design, simulation, layout, verification, or DfT tools
- Often released as **integrated flows or APIs**, must support standard formats (Verilog, GDSII, LEF/DEF) and operate within ecosystems (Cadence, Synopsys)

Solution Development in Semiconductors

Solution Types

Depending on the startup's nature, the solution might be:

C. ASIC/SoC Platforms

- Application-specific SoCs, often targeting verticals like automotive, AI, edge computing
- Must go beyond blocks and include **system-level performance metrics**, software stacks, and reference designs

D. Post-Fab / Manufacturing Tools

- Solutions for test automation, yield optimization, failure analysis
- Must integrate with fab data and be **highly robust and secure**

Solution Development in Semiconductors

Validation Requirements

In semiconductor B2B, a solution isn't taken seriously unless it is:

- **Technically sound**: Proven via simulation, test benches, and (ideally) tape-out results
- **Integratable**: Easy to adopt into existing workflows and toolchains
- **Benchmarkable**: Measurable performance vs. incumbent solutions (PPA, time-to-signoff, etc.)
- **Secure**: Protected against IP theft, supports licensing models
- **Documented**: Includes data sheets, app notes, and support for onboarding

"Your first customer is also your first validator.
Treat them like a co-developer, not a buyer."

Solution Development in Semiconductors

Minimum Viable Product (MVP) in Semiconductors

Your MVP might be:

- A **simulation model** with performance curves and integration examples
- A **taped-out test chip** on MPW (multi-project wafer)
- An **EDA plugin** that automates part of the flow (e.g., routing, verification coverage, parasitic extraction)
- A joint development agreement (JDA) with a lead customer

But it must always show proof of value — in time saved, yield improved, cost reduced, or performance unlocked.

Solution Development in Semiconductors

Iterate with Real Customers

- Early adopters are often found in **innovative teams** within large companies (e.g., R&D groups, tool flows engineers)
- Iteration happens through:
  - Evaluation licenses
  - NDA-protected beta deployments
  - Joint R&D or reference design programs

Solution development in semiconductors is customer-driven engineering — not speculative prototyping.

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Competitive Positioning in the Ecosystem

The Nature of Competition in Semiconductors

- You're not just competing on **features** or **price** — you're competing on **trust**, **performance**, **integration**, and **roadmap alignment**.
- Your competitors are likely entrenched incumbents (e.g., **Synopsys, Cadence, ARM, TSMC IP**, or internal teams at Apple/Nvidia).
- Often, the competition is **"do nothing"** — teams stick with inefficient tools or outdated IP because of inertia or integration risk.

"In semiconductors, adoption = risk.

Startups win only when the benefit clearly outweighs the risk of change."

Competitive Positioning in the Ecosystem

What Positioning Really Means

Competitive positioning answers the question:

"Why would a risk-averse customer choose your solution over a trusted incumbent or their in-house team?"

To answer that, a startup must show:

- **Clear, measurable edge**: PPA gains, design time saved, yield improved
- **Domain fit**: Deep alignment with the customer's use case and flow
- **Ecosystem compatibility**: Seamless integration with foundries, tools, formats, etc.

Competitive Positioning in the Ecosystem

Positioning Levers in the Semiconductor Context

A startup doesn’t have to be better at everything — but it must be clearly better at something that matters to the customer.

Lever	What It Means in Semi	Example
Performance Advantage	Faster, smaller, lower power, higher yield	IP block that uses 30% less area
Time Advantage	Accelerates design cycles or signoff	Tool that reduces verification by 40%
Integration & Compatibility	Works with industry-standard flows and foundry kits	EDA tool that plugs into Synopsys flow and supports TSMC PDKs
Silicon Proven	Already validated in tape-out or silicon	Customer tape-out on MPW shuttle with success
Security/Trust	Compliance (ISO 26262, automotive, IP protection)	Proven IP in functional safety environments
Customer Support	Customization, onboarding, rapid support	Known for “white glove” onboarding for Tier 1 customers

Competitive Positioning in the Ecosystem

Sustainable Differentiation (Building a Moat)

- **Design Complexity**: Proprietary architectures or ultra-high performance IP
- **Data Lock-in**: Tools that improve over time with usage (e.g., ML-enhanced DRC).
- **Ecosystem Embedding**: Deep integrations with foundry PDKs or vendor flows
- **Switching Cost**: Replacing your solution would break the customer's flow or risk performance.
- **Certification**: Automotive, medical, or aerospace certifications create strong entry barriers.

Competitive Positioning in the Ecosystem

Frameworks for Analyzing Positioning

- **Value Proposition Canvas** (focus on customer pains and gains)
- **Strategy Canvas** (compare feature performance across competitors)
- **Perceptual Map** (e.g., plot cost vs. performance; or flexibility vs. integration)

Competitive Positioning in the Ecosystem

Value Proposition Canvas

(focus on customer pains and gains is typically visualized as a two-part diagram:)

The **Right Side** is the **Customer Profile** — it defines the **target customer**: their needs, pain points, and desires.

The **Left Side** is the **Value Map** — it defines your **solution** and how it responds to those needs.

The goal is to ensure a **tight fit** between:

- the **customer's pains and jobs**
- and your **pain relievers and gain creators**

A perfect fit happens when your product solves a critical customer job, eliminates key pains, and adds meaningful gains.

Competitive Positioning in the Ecosystem

Example Customer Profile

Component	What it is	Example (for a semiconductor design team)
Customer Jobs	What they are trying to do	Tape out a SoC, integrate IP, meet timing/power goals
Pains	What frustrates or blocks them	Tools are slow, IP doesn’t port well, verification is tedious
Gains	What they wish they had	Faster tape-out, better tooling, support from experts

Competitive Positioning in the Ecosystem

Example Value Map

Component	What it is	Example (for a verification startup)
Products & Services	What you offer	AI-driven verification tool, pre-verified IP blocks
Pain Relievers	How you reduce their pain	Cuts verification time, improves coverage, avoids bugs
Gain Creators	How you deliver extra value	Better team productivity, shorter time-to-market

Competitive Positioning in the Ecosystem

Strategy Canvas

(compare feature performance across competitors)

Purpose

- Visualize how your startup compares to incumbents or substitutes
- Identify over-served, under-served, and uncontested value attributes
- Focus your differentiation on what truly matters to target customers

Competitive Positioning in the Ecosystem

Identify Key Factors of Competition

(For a semiconductor B2B context (IP, EDA, chiplets, ASIC platforms), these are common value dimensions:)

Value Factor	Description
Performance (PPA)	Power, performance, area efficiency
Toolchain Integration	Compatibility with Cadence, Synopsys, TSMC, etc.
Time-to-Integration	How quickly the solution can be deployed
Verification Coverage	Thoroughness and automation of testing
Customization	Ability to tailor the product to specific customer needs
Support & Service	Responsiveness, onboarding, SLAs
Cost	Total cost of adoption (licenses, NRE, risk)
Innovation / Novelty	New architectures, AI-driven flows, chiplets, etc.

Competitive Positioning in the Ecosystem

Key Takeaway for Founders

Don’t try to beat incumbents at their own game.
Instead, find the inefficiencies they overlook — and win there.

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Interactive Exercise: Problem Hunt

Task: Identify 3 real-world problems in semi design/manufacturing

- Where are bottlenecks?
- Who suffers the pain?
- What would make the process 10x better?

Pitch the Problem

Each team presents:

- The problem
- Who it affects
- Evidence that it matters
- Consider investor criteria discussed earlier.

Wrapping Up

- ✓ Semiconductor B2B startups face unique challenges
- ✓ Problems must be urgent, measurable, and well understood
- ✓ MVPs must inspire confidence through technical rigor
- ✓ Sustainable moats = integration, trust, and domain expertise

Thank You!

Now, time for the Power of Interaction!

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