IC Synthesis and optimization

Lab 7: Physical synthesis: Signoff

Objective
To study Signoff process using ICV tools.

Theoretical part:

IC Validator (ICV) is a signoff tool for DRC, LVS and ANT checks.

StarRC is a next-generation layout parasitic extraction tool that extracts connected databases. StarRC can be used at any physical design cycle stage to extract accurate parasitic. StarRC is the EDA industry's standard for parasitic extraction. StarRC provides silicon-accurate and high-performance extraction solution for SoC, custom digital, analog/mixed signal (AMS and memory IC designs).

PrimeTime is a full-chip, gate-level static timing analysis tool that is an essential part of the design and analysis flow for today's large chip designs. PrimeTime validates the timing performance of a design by checking all possible paths for timing violations, without using logic simulation or test vectors.

Practical part
Move to directory lab7/work.

1 Invoke and set-up ICC II.

```
icc2_shell -gui -64
source ../../common/common.tcl
open_lib ${ARC_TOP}
open_block ${DESIGN_NAME}_6_complete
```

2 Set-up ICV to run signoff DRC checks.

For ICV environment setup the following options must be used.

```
set_app_options -name signoff.check_drc.runset \
-value ${icv_drc_runset}
set_app_options -name signoff.check_drc.max_errors_per_rule \
-value 1000
set_app_options -name signoff.check_drc.run_dir \
-value "./signoff_drc_run/"
set_app_options -name signoff.physical.layer_map_file \
-value ${Gds_map_file}
```

To run DRC *signoff_check_drc* command is used.

```
signoff_check_drc
```

Note that ICV version must be later than ICC II version.

To check LVS errors, run check_lvs command.

Use the error browser to visualize any routing violations in the GUI that may have been left over. On the top toolbar,select the button for the error browser.(Fig.1)

Fig.17. Error browser

3 Run timing analysis

```
Source ../../lab6_pnr/scripts/mcmm.tcl

set_app_options -name time.enable_ccs_rcv_cap -value true

set_app_options -name extract.starrc_mode -value false

report_constraints -all_violators
```

Exercise:

1. Define a clock uncertainty for hold of 50ps by “set_clock_uncertainty -hold 0.05 [all_clocks]”. Fix all timing violations.