# TECHNOLOGY CHARACTERIZATION WORKSHOP

## Module 1

# Contents

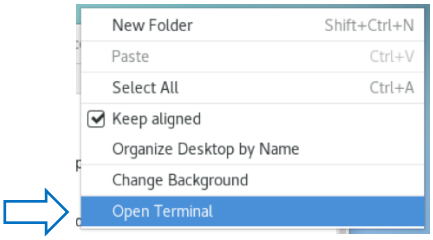
# 1. Revision History

| Version | Date | Authors | Comments |
|---|---|---|---|
| 1.0 | 2025/06/23 | Renesas Team | • Initial version |

# 2. Create working library

## 2.1. Open new Mate Terminal

Right click on desktop and open a new Terminal.




## 2.2. Select the Project directory

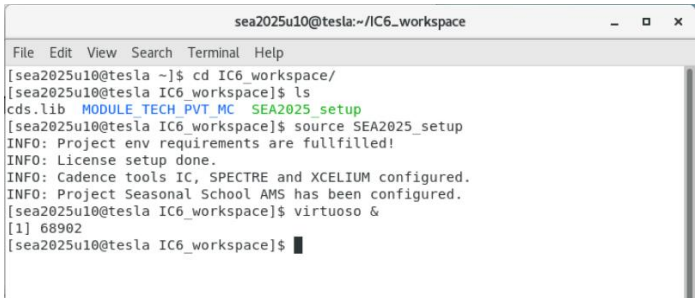
- *cd IC6_workspace*

## 2.3. Load environment variables

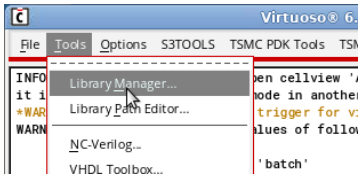
- source SEA2025_setup

## 2.4. Launch the Cadence Virtuoso

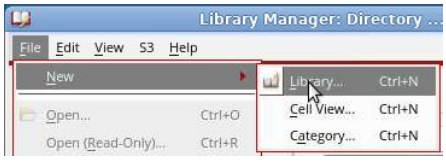
- virtuoso &




## 2.5. Open library manager



## 2.6. Create new working library

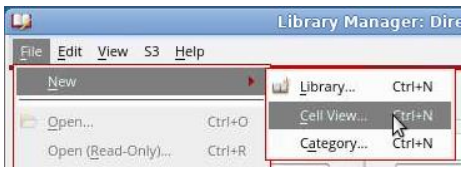



Give a suitable name to your working library (on below examples the name "*AMSdesign2025*" was used) and attach it to and existing technology library.

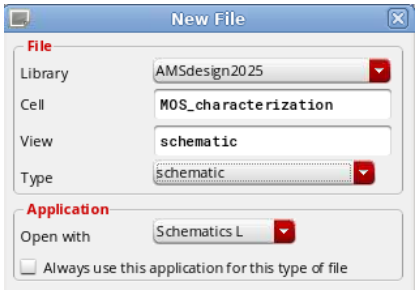

Select "*tsmcN28*" from the list and click OK.

# 3. MOS Parameter Characterization

## 3.1. Create a new schematic view

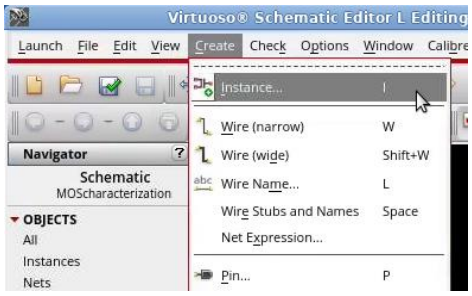


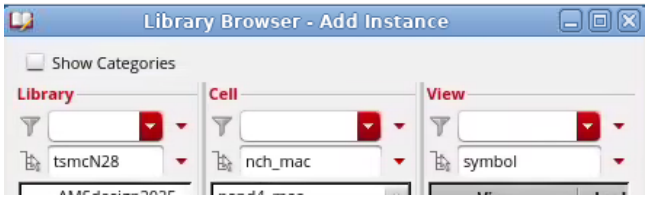

Give a suitable name to your schematic (on below examples the name "MOS_characterization" was used).




## 3.2. Add devices

Instance a core voltage NMOS ("nch_mac") and PMOS ("pch_mac"), and DC voltage sources like the schematic below.
Rename the NMOS instance to "T_NMOS" and the PMOS instance to "T_PMOS", for later use.

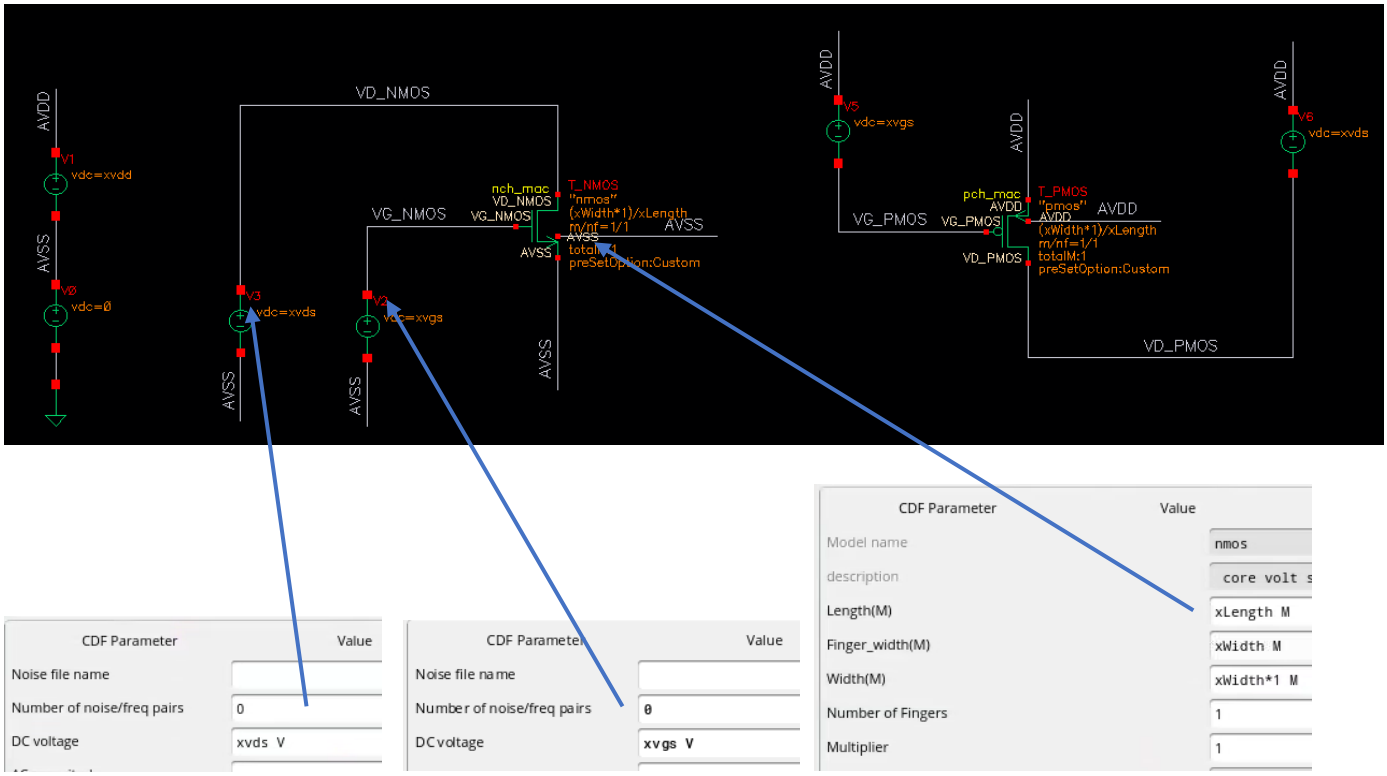



| Instance | Library | Cell | View |
|---|---|---|---|
| NMOS | tsmcN28 | nch_mac | symbol |
| PMOS | tsmcN28 | pch_mac | symbol |
| DC voltage source | analogLib | vdc | symbol |
| ground | basic | gnd | symbol |

Add variable names to DC voltages sources values, and to length and width of transistors to be used later for parameters variations. See examples below:

h

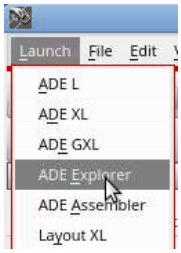



Alternatively, you can copy the following pre-edited schematic to your library:

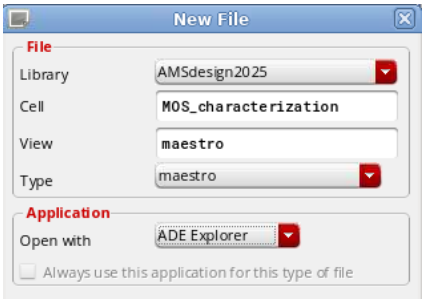
| Library | Cell | View |
|---|---|---|
| MODULE_TECH_PVT_MC | MOS_characterization | schematic |

## 3.3. Create a new Maestro Analog Design Environment (ADE Explorer)

On schematic launch the Maestro ADE Explorer environment.

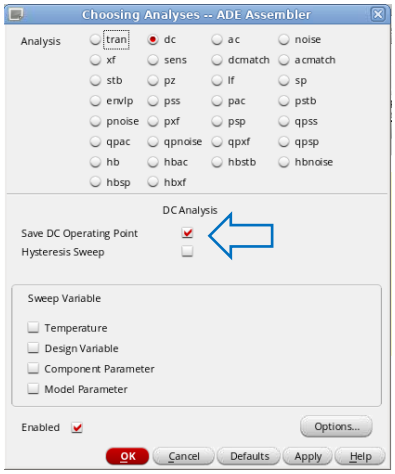




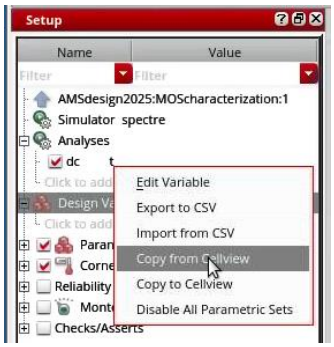


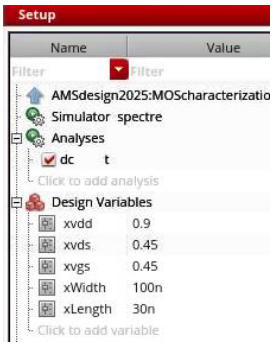
## 3.4. Select analysis and define variable values

Select "*dc*" analysis and "Save DC Operating Point" check box.



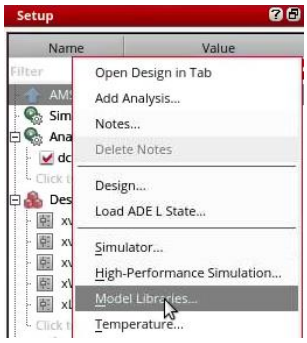

Copy variables from schematic and double click on the left side of the variable to edit their values. See example below.

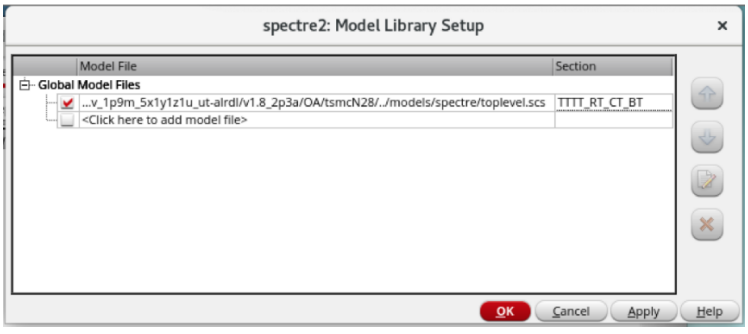



## 3.5. Edit Model Libraries path and Corner Section

Add the below model libraries path to "Global Model Files" and select "TTTT_RT_CT_BT" as corner section:

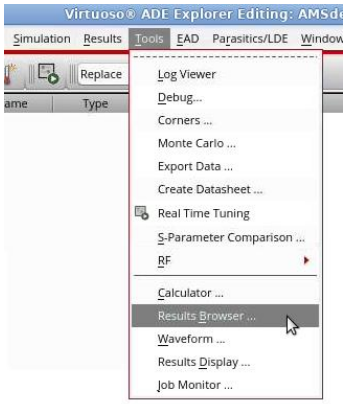


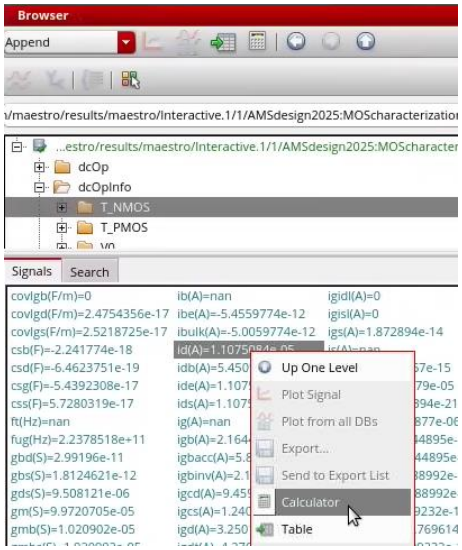

Models file path: /DataHDD/tsmc/28n_rf_ull_hpc_plus_0p9v_1p8v_1p9m_5x1y1z1u_ut-alrdl/v1.8_2p3a/OA/tsmcN28/../models/spectre/toplevel.scs

## 3.6. Run Simulation and see results

Hit the ▶ to run the simulation and open the “Results Browser”.

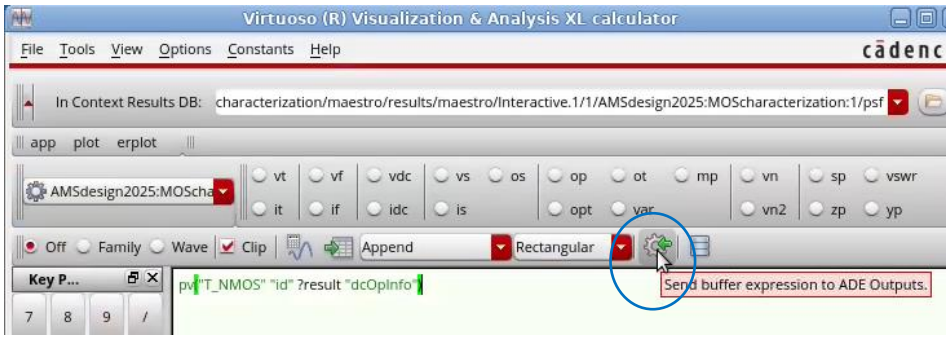



On Results Browser select one transistor DC operating point parameter and send it to calculator.



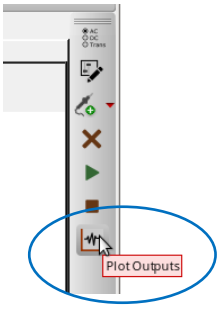

Right click over any transistor parameter value to open the dialog box

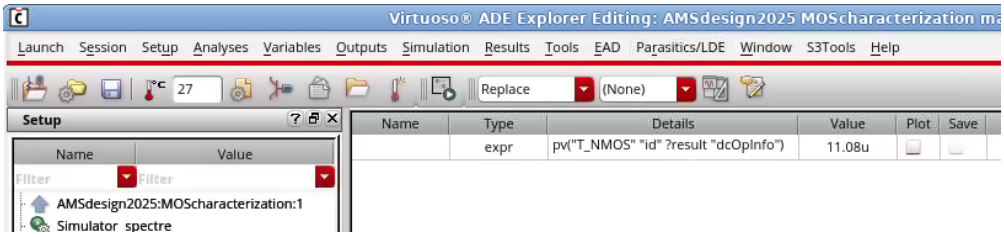
Once on calculator send it to Maestro ADE to be calculated every time the simulation is run.




Do the above steps for every parameter you want to observe.

Refresh the ADE outputs plot and confirm the resulting values are matched with the results browser. See example below:




Every time a new simulation is run the saved expression will be calculated and their results plotted on ADE outputs results.

## 3.7. Load a pre-defined list of measurements

Import the below pre-defined measures file and refresh the ADE outputs plot.

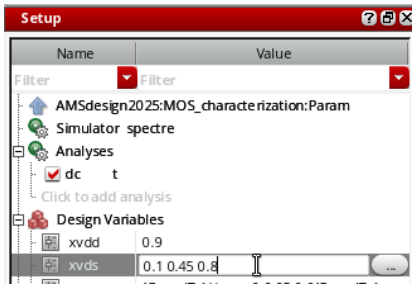

Pre-defined measurements file path:
~/IC6_workspace/MODULE_TECH_PVT_MC/
outputs_AMSdesign2025_MOS_characterization_maestro_params.csv

Example of measured results:

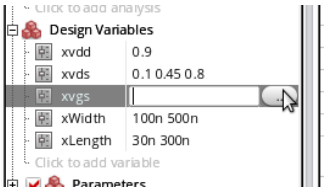
| Name | Type | Details | Value | Plot |
|---|---|---|---|---|
| VGS | expr | (v("/VG_NMOS" ?result "dcOp") - v("/AVSS" ?result "dcOp")) | 450m | |
| VDS | expr | (v("/VD_NMOS" ?result "dcOp") - v("/AVSS" ?result "dcOp")) | 450m | |
| Id_NMOS | expr | pv("T_NMOS" "id" ?result "dcOpInfo") | 11.08u | |
| GmoverId_NMOS | expr | (pv("T_NMOS" "gm" ?result "dcOpInfo") / pv("T_NMOS" "id" ?result "dcOpInfo")) | 9.004 | |
| Vdsat_NMOS | expr | pv("T_NMOS" "vdsat" ?result "dcOpInfo") | 169.3m | |
| Vth_NMOS | expr | pv("T_NMOS" "vth" ?result "dcOpInfo") | 390.3m | |
| Gm_NMOS | expr | pv("T_NMOS" "gm" ?result "dcOpInfo") | 99.72u | |
| Gds_NMOS | expr | pv("T_NMOS" "gds" ?result "dcOpInfo") | 9.508u | |
| Cgg_NMOS | expr | pv("T_NMOS" "cgg" ?result "dcOpInfo") | 70.92a | |
| Cds_NMOS | expr | pv("T_NMOS" "cds" ?result "dcOpInfo") | 458.6z | |
| Cgd_NMOS | expr | pv("T_NMOS" "cgd" ?result "dcOpInfo") | -24.87a | |
| Cgs_NMOS | expr | pv("T_NMOS" "cgs" ?result "dcOpInfo") | -41.79a | |
| Ig_NMOS | expr | pv("T_NMOS" "igdt" ?result "dcOpInfo") | 42.76f | |
| Id_PMOS | expr | pv("T_PMOS" "id" ?result "dcOpInfo") | -2.855u | |
| GmoverId_PMOS | expr | abs((pv("T_PMOS" "gm" ?result "dcOpInfo") / pv("T_PMOS" "id" ?result "dcOpInfo"))) | 15.49 | |
| Vdsat_PMOS | expr | pv("T_PMOS" "vdsat" ?result "dcOpInfo") | -75.65m | |
| Vth_PMOS | expr | pv("T_PMOS" "vth" ?result "dcOpInfo") | -442.6m | |
| Gm_PMOS | expr | pv("T_PMOS" "gm" ?result "dcOpInfo") | 44.22u | |
| Gds_PMOS | expr | pv("T_PMOS" "gds" ?result "dcOpInfo") | 5.491u | |
| Cgg_PMOS | expr | pv("T_PMOS" "cgg" ?result "dcOpInfo") | 74.95a | |
| Cds_PMOS | expr | pv("T_PMOS" "cds" ?result "dcOpInfo") | 61.63z | |
| Cgd_PMOS | expr | pv("T_PMOS" "cgd" ?result "dcOpInfo") | -25.19a | |
| Cgs_PMOS | expr | pv("T_PMOS" "cgs" ?result "dcOpInfo") | -46.06a | |
| Ig_PMOS | expr | pv("T_PMOS" "igdt" ?result "dcOpInfo") | -64.96f | |

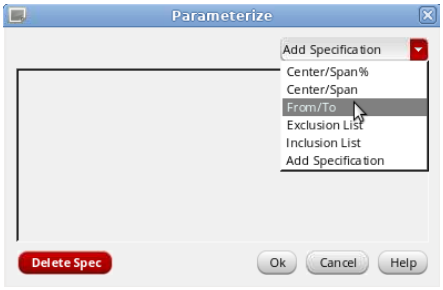
## 3.8. Add transistors parameters variations

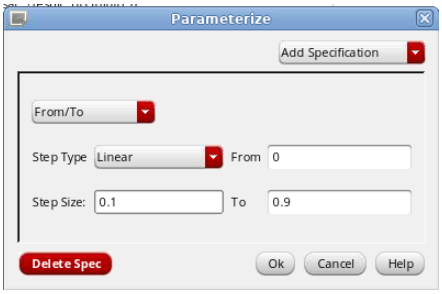
On ADE setup environment add more than one value to variables to enable the parametric simulations. ADE will cross all the values independently and run a simulation for each possible combination. See examples below:



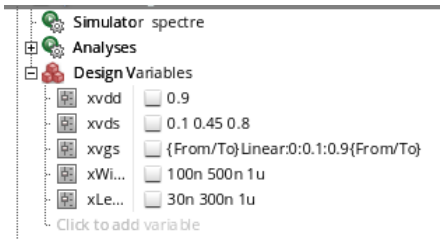

Add values directly to dialog box separated by spaces like the example on the left or open the “Parameterize” box as the example below.



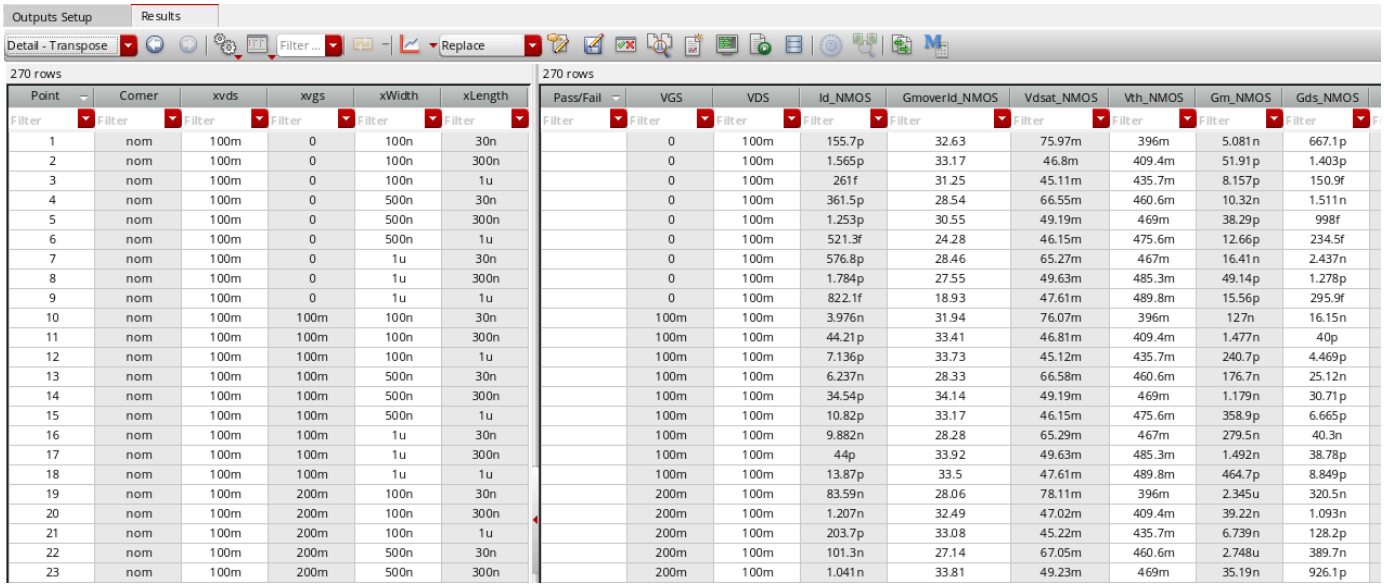



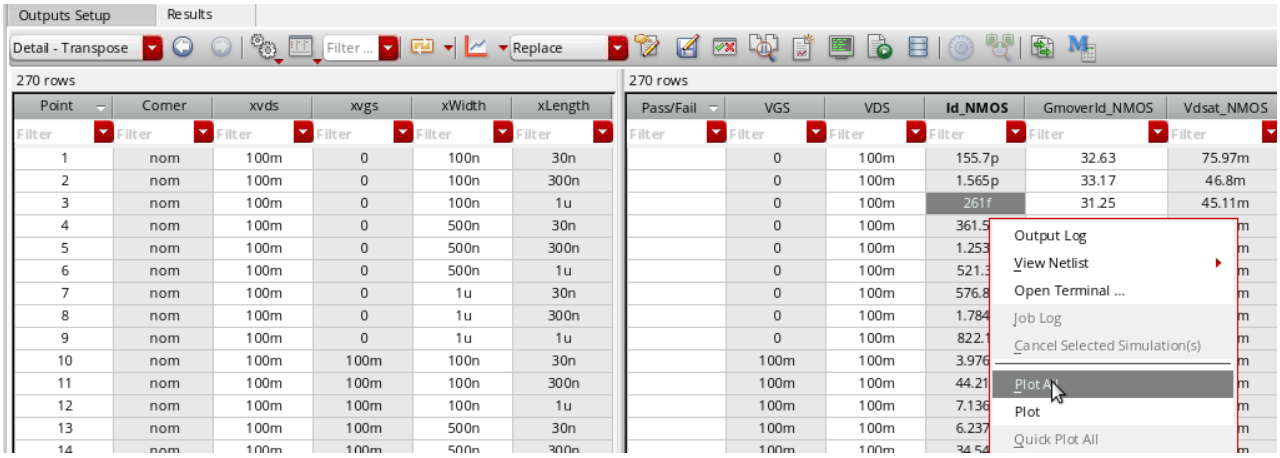

Example of parametric variables variations within accepted devices sizes and operating voltages:



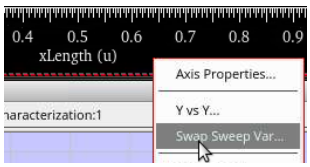

See below an example of simulation results table. Please note, for a broader visualization, the table has been presented on “Detail - Transpose” format.




To plot all the results of a measured parameter right click on one of the results and select “Plot All”.

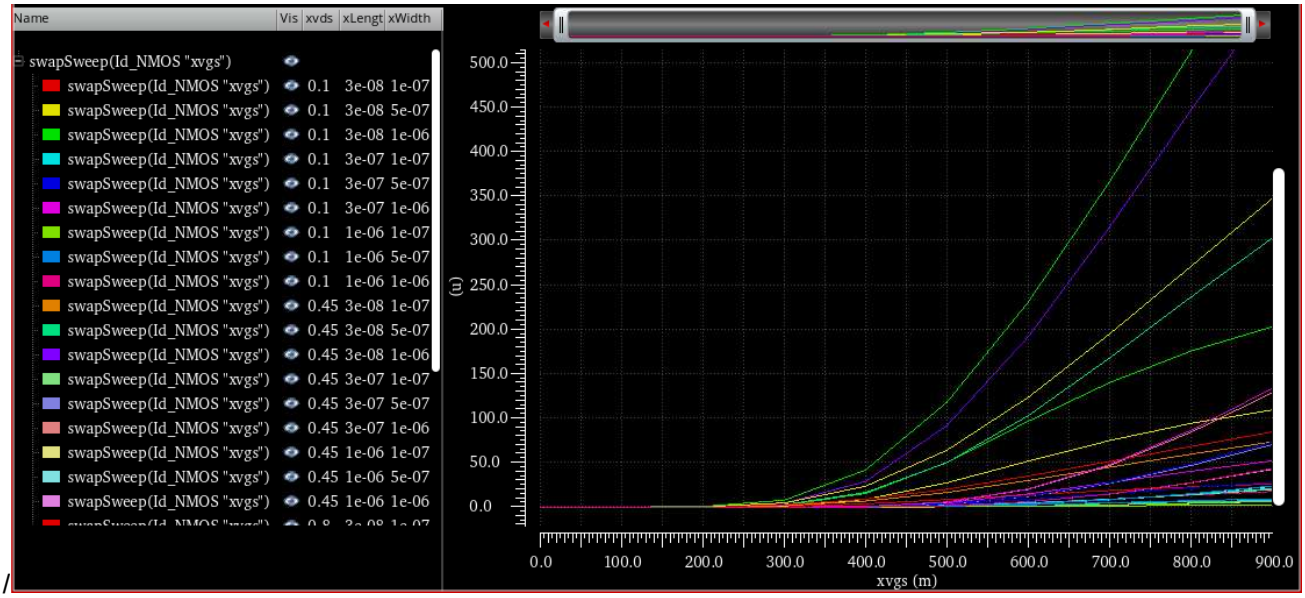



Please note, if X axis on plotted waveform is not Vgs voltage, change it by right click on the X axis and select “*Swap Sweep Var*” dialog box and change it to “xvgs” variable.

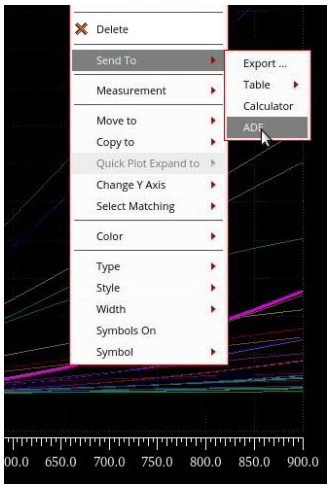




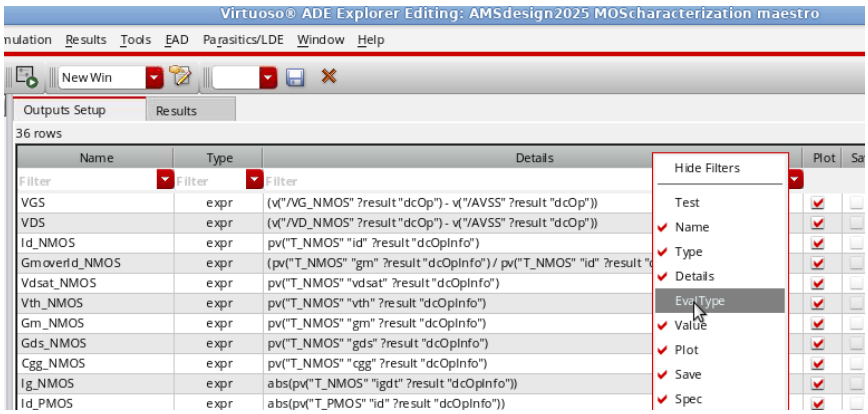
See a plot example below for NMOS drain current (vs) Vgs voltage simulation results for the different parametric values.



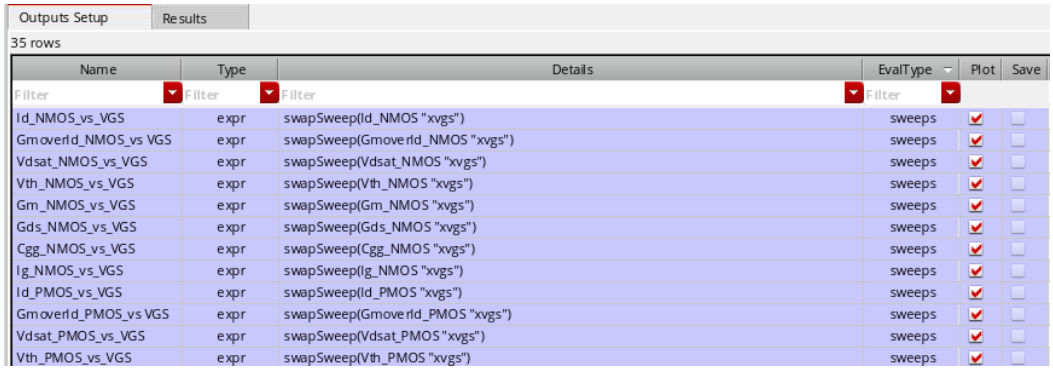

Plotted signals can be added to ADE by right click on a waveform → Send To → ADE. See the example below:




On ADE right click on the Details tab and make the “EvalType” column visible:



Double click on the “EvalType” box and change it from “point” to “Sweeps” to enable the post processing of the plots after all parametric simulations have been concluded for a correct plotting of results and refresh the results table. A more user-friendly name can be given to the plot. See some examples below:

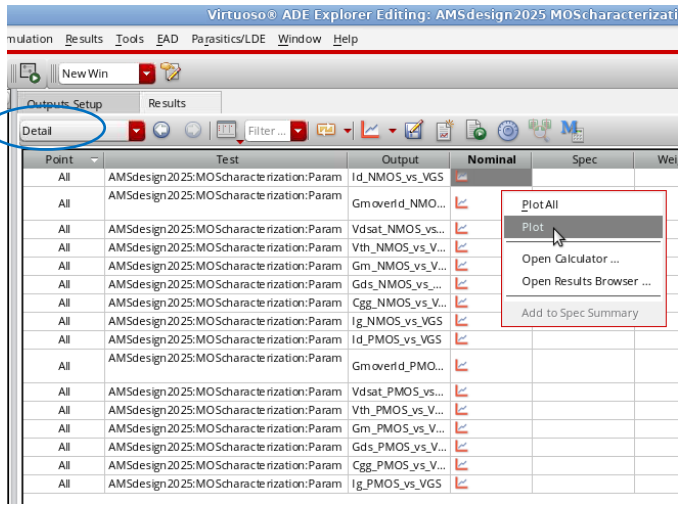

Outputs Setup | Results

35 rows

| Name | Type | Details | EvalType | Plot | Save |
|---|---|---|---|---|---|
| Id_NMOS_vs_VGS | expr | swapSweep(Id_NMOS "xvgs") | sweeps | ☑ | ☐ |
| GmoverId_NMOS_vs VGS | expr | swapSweep(GmoverId_NMOS "xvgs") | sweeps | ☑ | ☐ |
| Vdsat_NMOS_vs_VGS | expr | swapSweep(Vdsat_NMOS "xvgs") | sweeps | ☑ | ☐ |
| Vth_NMOS_vs_VGS | expr | swapSweep(Vth_NMOS "xvgs") | sweeps | ☑ | ☐ |
| Gm_NMOS_vs_VGS | expr | swapSweep(Gm_NMOS "xvgs") | sweeps | ☑ | ☐ |
| Gds_NMOS_vs_VGS | expr | swapSweep(Gds_NMOS "xvgs") | sweeps | ☑ | ☐ |
| Cgg_NMOS_vs_VGS | expr | swapSweep(Cgg_NMOS "xvgs") | sweeps | ☑ | ☐ |
| Ig_NMOS_vs_VGS | expr | swapSweep(Ig_NMOS "xvgs") | sweeps | ☑ | ☐ |
| Id_PMOS_vs_VGS | expr | swapSweep(Id_PMOS "xvgs") | sweeps | ☑ | ☐ |
| GmoverId_PMOS_vs VGS | expr | swapSweep(GmoverId_PMOS "xvgs") | sweeps | ☑ | ☐ |
| Vdsat_PMOS_vs_VGS | expr | swapSweep(Vdsat_PMOS "xvgs") | sweeps | ☑ | ☐ |
| Vth_PMOS_vs_VGS | expr | swapSweep(Vth_PMOS "xvgs") | sweeps | ☑ | ☐ |

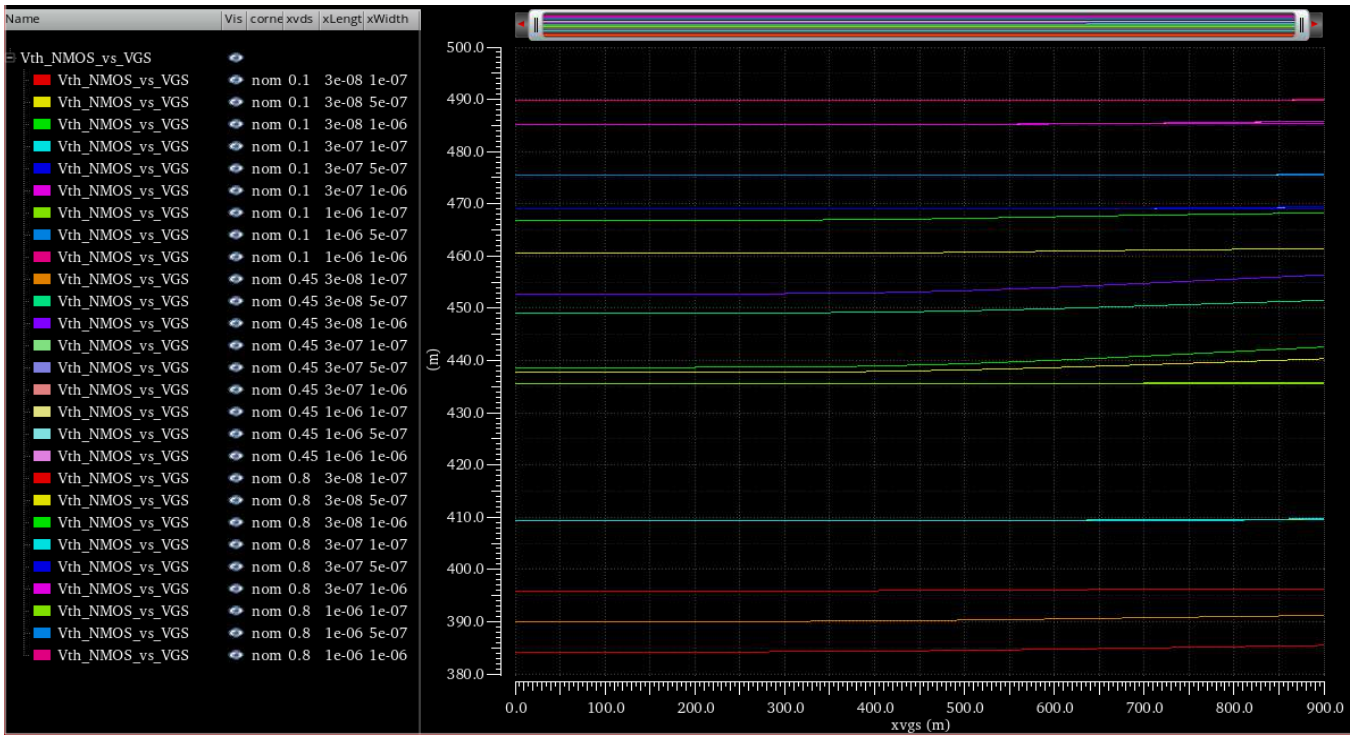
Alternatively, you can import the following pre-defined plots file:
~/IC6_workspace / MODULE_TECH_PVT_MC / outputs_AMSdesign2025_MOS_characterization_maestro_plots.csv

To plot the above expressions, change the visualization of results on ADE to “Detail” and plot the waveforms with right click on a result waveform icon, and then on Plot.

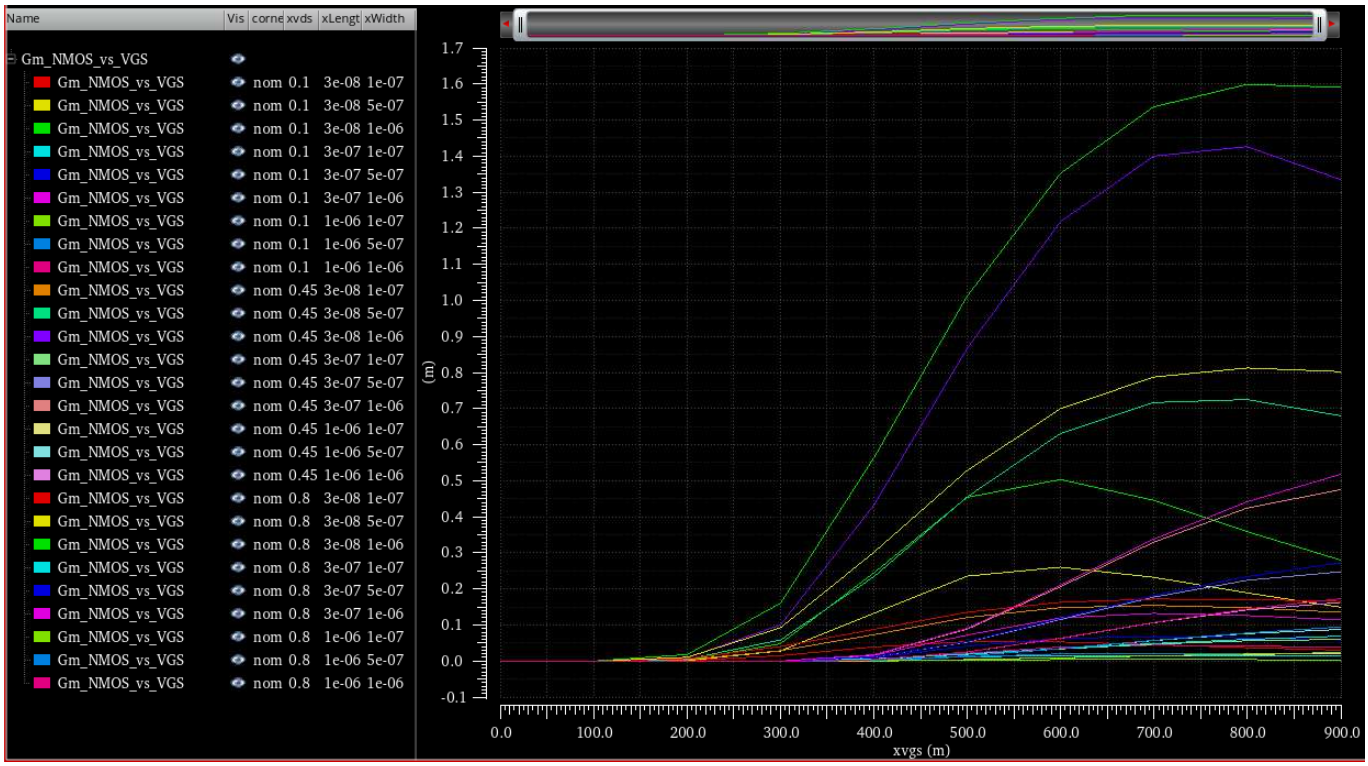



Example of plots from ADE expression simulation results table:

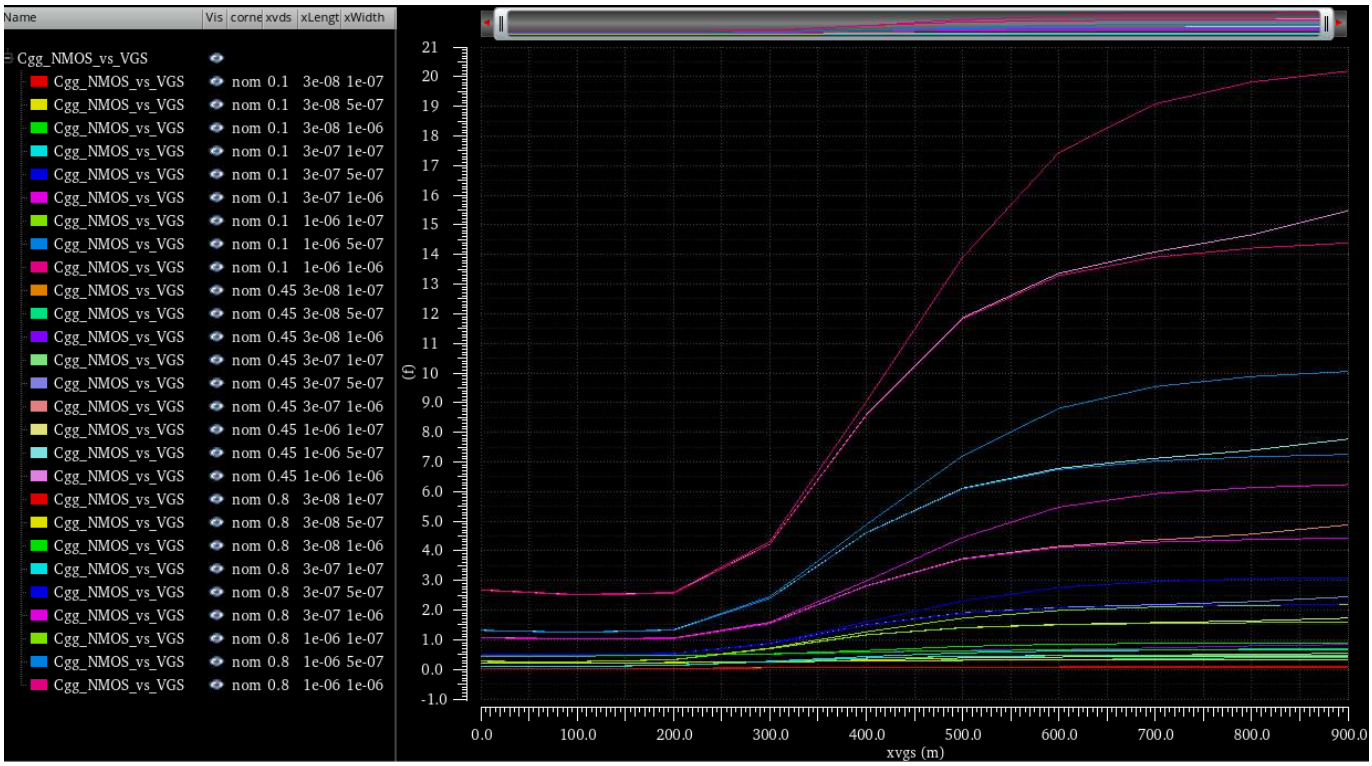
- NMOS Vth (vs) Vgs (Threshold voltage vs gate to source differential voltage)



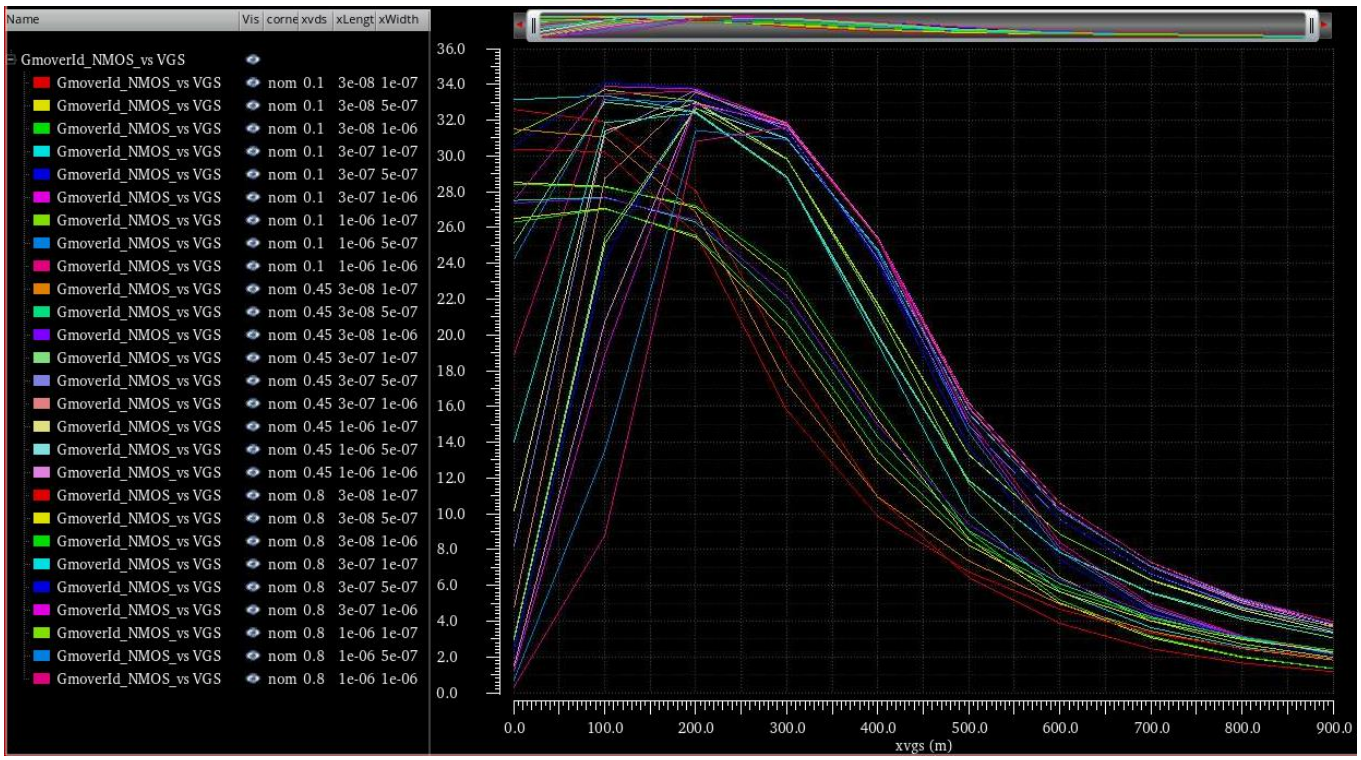

- NMOS Gm (vs) Vgs (Transconductance vs gate to source differential voltage)



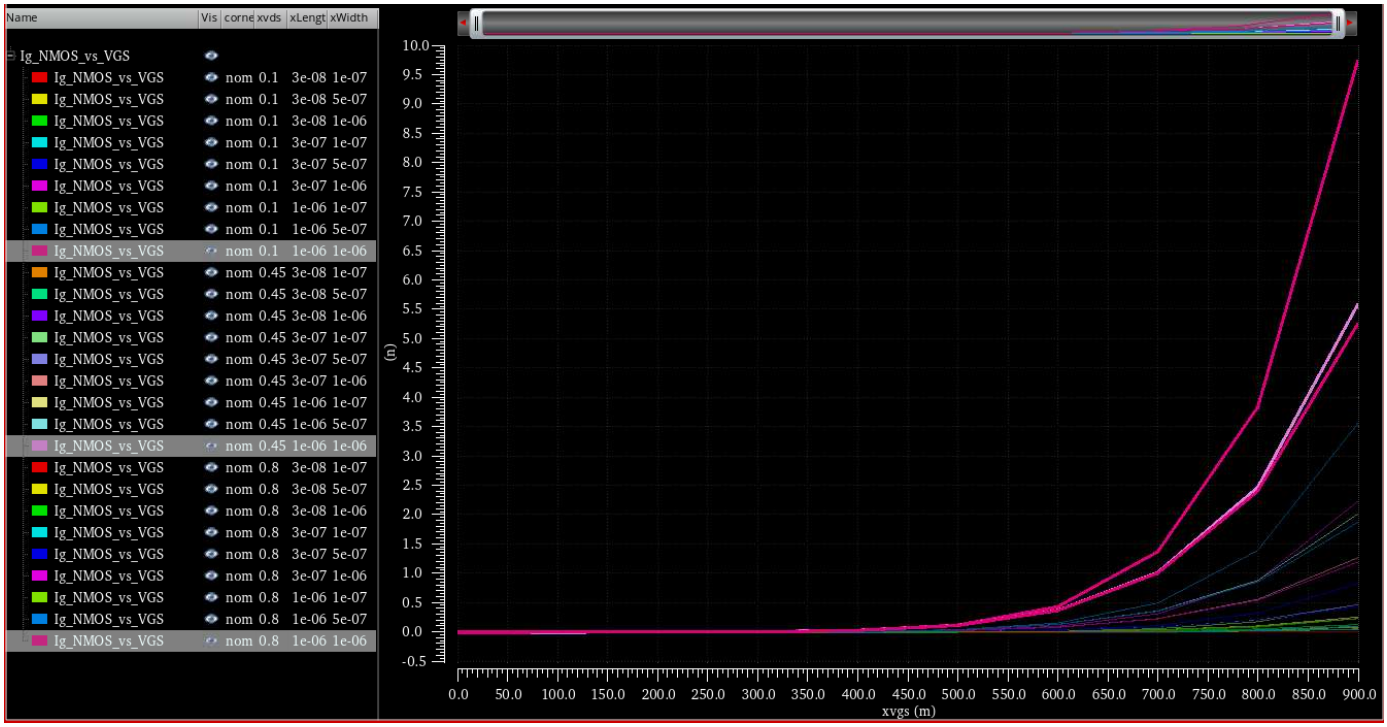
- NMOS Cgg (vs) Vgs (Total gate capacitance vs gate to source differential voltage)




- NMOS Gm/Id (vs) Vgs (Transconductance Efficiency vs gate to source differential voltage)

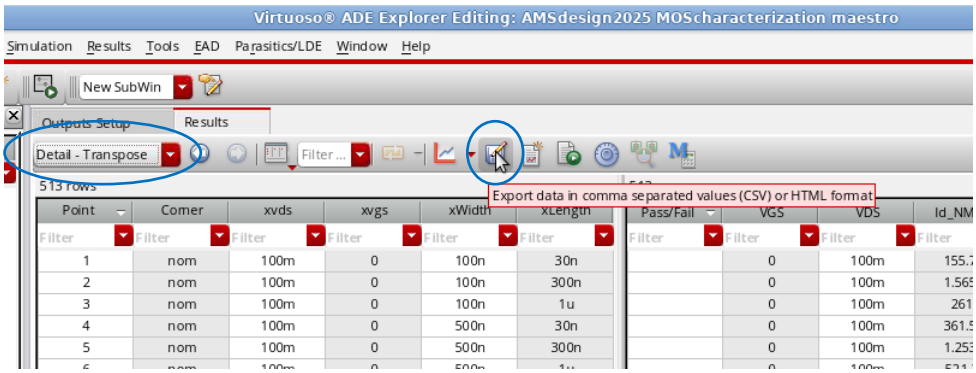


- NMOS Ig (vs) Vgs (gate leakage vs gate to source differential voltage)

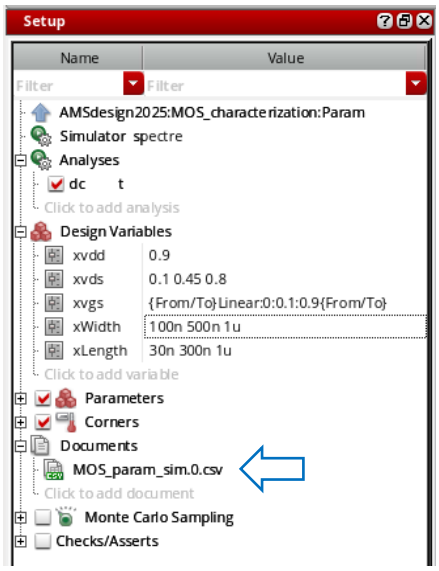



## 3.9. Save results to CSV file

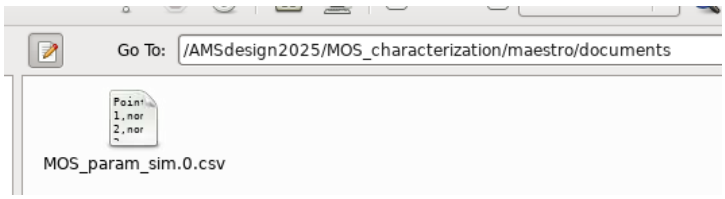
Simulation measured results can be saved on CSV file for post-simulation editing using for example Matlab, Excel, Octave, etc.



The saved CSV file can be accessed directly from the Maestro ADE on “Documents” tab.




Or alternatively through the file explorer on the following location:

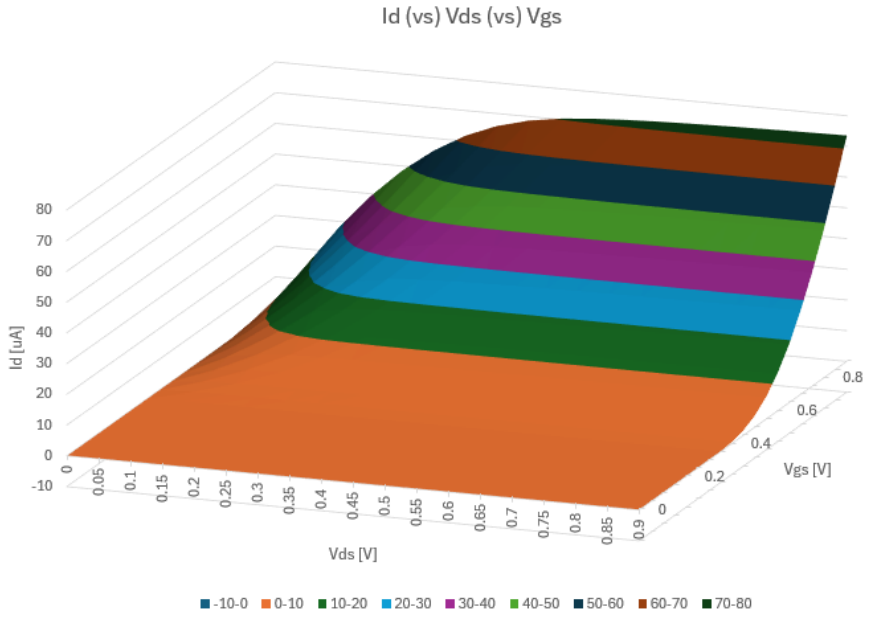



*<Library name> / <Testbench schematic design name> / maestro / documents / <csv filename>*

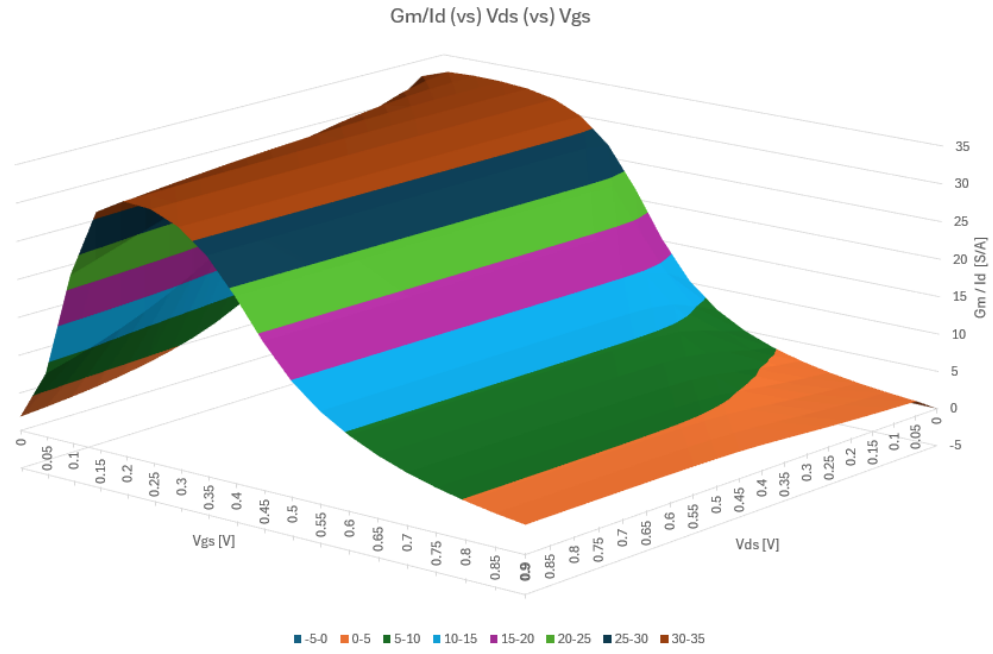
## 3.10. Example of post processing CSV data

On the example below the Id and Gm/Id of a NMOS transistor has been measured with a sweep of Vds and Vgs voltages on the range [0V ; 0.9V] in steps of 50mV independently. Results have been saved to CSV format, copied to Excel tool and the following 3D plots have been generated.

- Id (vs) Vds (vs) Vgs




- Gm / Id (vs) Vds (vs) Vgs



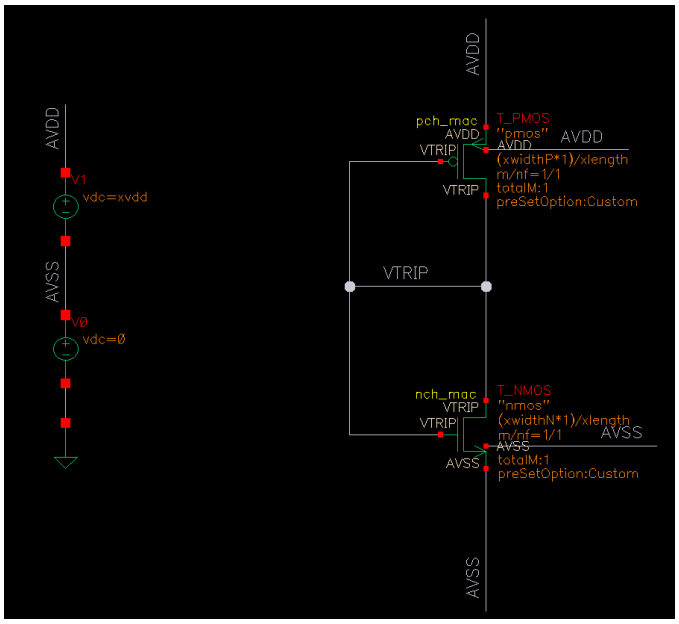
# 4. Diode connected inverter

## 4.1. Schematic

Copy the Diode Connected Inverter schematic from reference library.

| Library | Cell | View |
|---|---|---|
| MODULE_TECH_PVT_MC | Dio_con_Inverter | schematic |

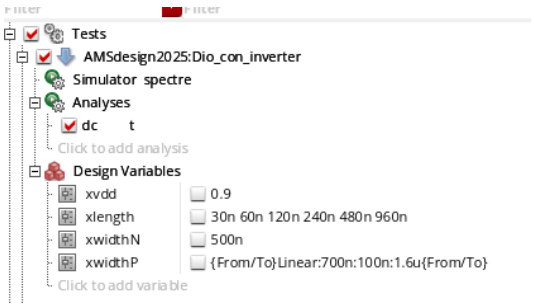
The objective of this testbench is to measure the VTRIP voltage and transistors “dc operating point” results for different lengths and widths.




## 4.2. Maestro ADE simulation environment

Create a new Maestro ADE simulation environment. Configure the model’s library and select “TTTT_RT_CT_BT” section.

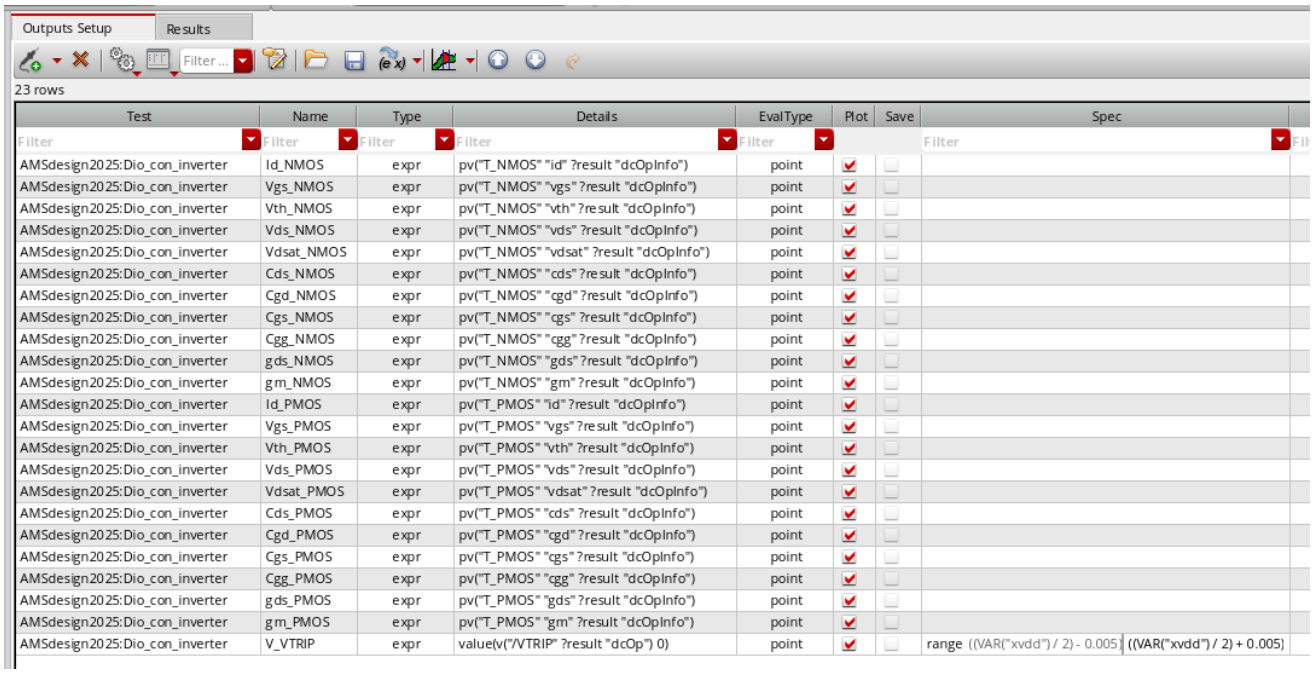
Select “dc” simulation and “Save DC Operating Point” check box (if necessary, revisit point 3 above for more details). Edit the devices variables as below example:




Please note: the Width of NMOS has been kept stable to reduce the number of simulation iterations.

Import the following pre-defined measures file:
~/IC6_workspace / MODULE_TECH_PVT_MC / outputs_AMSdesign2025_Dio_con_Inverter_maestro.csv

The Maestro ADE should be like the example below:



Outputs Setup | Results

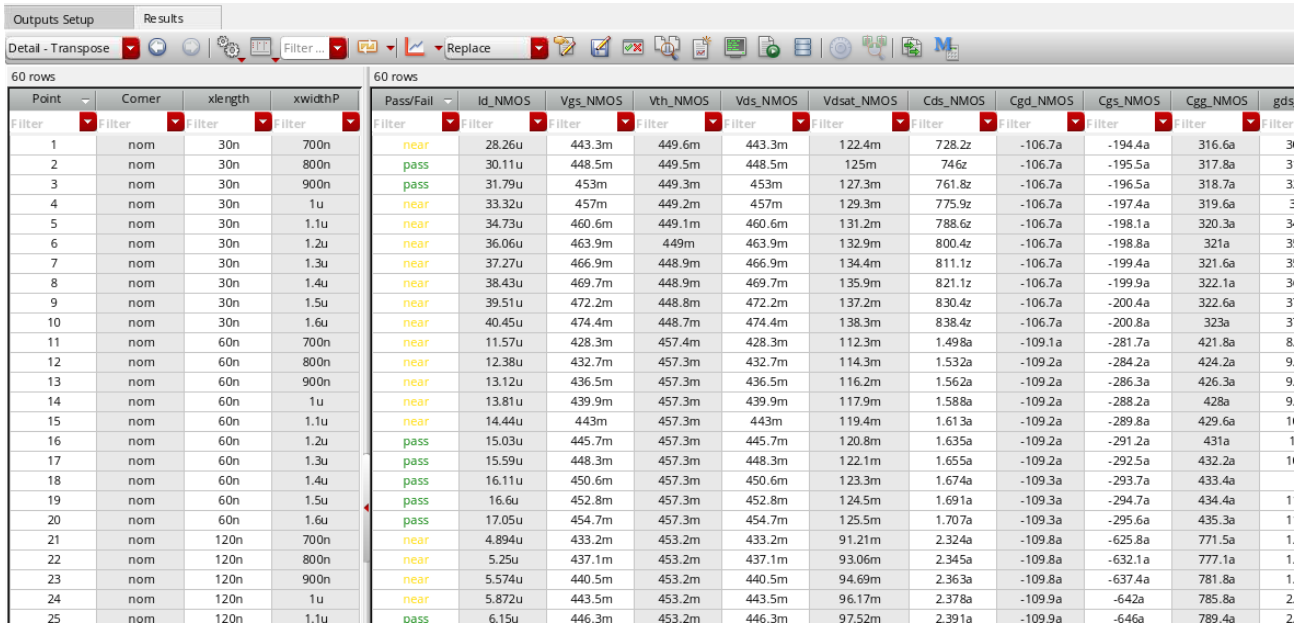
23 rows

| Test | Name | Type | Details | EvalType | Plot | Save | Spec |
|---|---|---|---|---|---|---|---|
| AMSdesign2025:Dio_con_inverter | Id_NMOS | expr | pv("T_NMOS" "id" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vgs_NMOS | expr | pv("T_NMOS" "vgs" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vth_NMOS | expr | pv("T_NMOS" "vth" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vds_NMOS | expr | pv("T_NMOS" "vds" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vdsat_NMOS | expr | pv("T_NMOS" "vdsat" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cds_NMOS | expr | pv("T_NMOS" "cds" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cgd_NMOS | expr | pv("T_NMOS" "cgd" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cgs_NMOS | expr | pv("T_NMOS" "cgs" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cgg_NMOS | expr | pv("T_NMOS" "cgg" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | gds_NMOS | expr | pv("T_NMOS" "gds" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | gm_NMOS | expr | pv("T_NMOS" "gm" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Id_PMOS | expr | pv("T_PMOS" "id" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vgs_PMOS | expr | pv("T_PMOS" "vgs" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vth_PMOS | expr | pv("T_PMOS" "vth" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vds_PMOS | expr | pv("T_PMOS" "vds" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Vdsat_PMOS | expr | pv("T_PMOS" "vdsat" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cds_PMOS | expr | pv("T_PMOS" "cds" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cgd_PMOS | expr | pv("T_PMOS" "cgd" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cgs_PMOS | expr | pv("T_PMOS" "cgs" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | Cgg_PMOS | expr | pv("T_PMOS" "cgg" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | gds_PMOS | expr | pv("T_PMOS" "gds" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | gm_PMOS | expr | pv("T_PMOS" "gm" ?result "dcOpInfo") | point | ✓ | | |
| AMSdesign2025:Dio_con_inverter | V_VTRIP | expr | value(v("/VTRIP" ?result "dcOp") 0) | point | ✓ | | range ((VAR("xvdd") / 2) - 0.005) ((VAR("xvdd") / 2) + 0.005) |

A spec has been set to V_VTRIP measurement to better identify the transistors sizes that are closer to the desired V_VTRIP = AVDD / 2 = 450mV (all results within a margin of 450±5mV will appear as green color).

## 4.3. Simulation results

Run the nominal simulation. See below example of simulation results:



Outputs Setup | Results

Detail - Transpose

60 rows

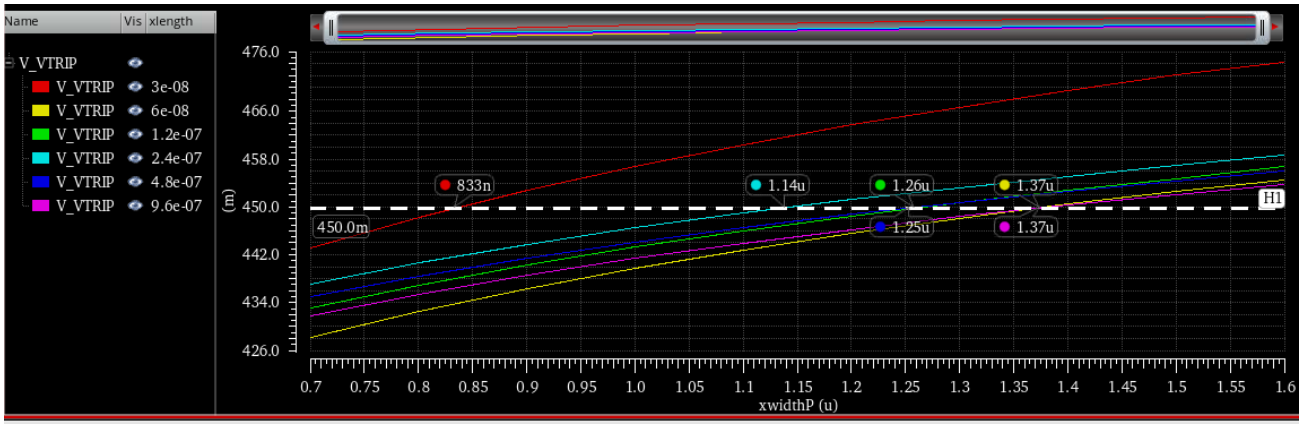
| Point | Corner | xlength | xwidthP |
|---|---|---|---|
| 1 | nom | 30n | 700n |
| 2 | nom | 30n | 800n |
| 3 | nom | 30n | 900n |
| 4 | nom | 30n | 1u |
| 5 | nom | 30n | 1.1u |
| 6 | nom | 30n | 1.2u |
| 7 | nom | 30n | 1.3u |
| 8 | nom | 30n | 1.4u |
| 9 | nom | 30n | 1.5u |
| 10 | nom | 30n | 1.6u |
| 11 | nom | 60n | 700n |
| 12 | nom | 60n | 800n |
| 13 | nom | 60n | 900n |
| 14 | nom | 60n | 1u |
| 15 | nom | 60n | 1.1u |
| 16 | nom | 60n | 1.2u |
| 17 | nom | 60n | 1.3u |
| 18 | nom | 60n | 1.4u |
| 19 | nom | 60n | 1.5u |
| 20 | nom | 60n | 1.6u |
| 21 | nom | 120n | 700n |
| 22 | nom | 120n | 800n |
| 23 | nom | 120n | 900n |
| 24 | nom | 120n | 1u |
| 25 | nom | 120n | 1.1u |

60 rows

| Pass/Fail | Id_NMOS | Vgs_NMOS | Vth_NMOS | Vds_NMOS | Vdsat_NMOS | Cds_NMOS | Cgd_NMOS | Cgs_NMOS | Cgg_NMOS | gds |
|---|---|---|---|---|---|---|---|---|---|---|
| near | 28.26u | 443.3m | 449.6m | 443.3m | 122.4m | 728.2z | -106.7a | -194.4a | 316.6a | 3 |
| pass | 30.11u | 448.5m | 449.5m | 448.5m | 125m | 746z | -106.7a | -195.5a | 317.8a | 3 |
| pass | 31.79u | 453m | 449.3m | 453m | 127.3m | 761.8z | -106.7a | -196.5a | 318.7a | 3 |
| near | 33.32u | 457m | 449.2m | 457m | 129.3m | 775.9z | -106.7a | -197.4a | 319.6a | 3 |
| near | 34.73u | 460.6m | 449.1m | 460.6m | 131.2m | 788.6z | -106.7a | -198.1a | 320.3a | 3 |
| near | 36.06u | 463.9m | 449m | 463.9m | 132.9m | 800.4z | -106.7a | -198.8a | 321a | 3 |
| near | 37.27u | 466.9m | 448.9m | 466.9m | 134.4m | 811.1z | -106.7a | -199.4a | 321.6a | 3 |
| near | 38.43u | 469.7m | 448.9m | 469.7m | 135.9m | 821.1z | -106.7a | -199.9a | 322.1a | 3 |
| near | 39.51u | 472.2m | 448.8m | 472.2m | 137.2m | 830.4z | -106.7a | -200.4a | 322.6a | 3 |
| near | 40.45u | 474.4m | 448.7m | 474.4m | 138.3m | 838.4z | -106.7a | -200.8a | 323a | 3 |
| near | 11.57u | 428.3m | 457.4m | 428.3m | 112.3m | 1.498a | -109.1a | -281.7a | 421.8a | 8 |
| near | 12.38u | 432.7m | 457.3m | 432.7m | 114.3m | 1.532a | -109.2a | -284.2a | 424.2a | 9 |
| near | 13.12u | 436.5m | 457.3m | 436.5m | 116.2m | 1.562a | -109.2a | -286.3a | 426.3a | 9 |
| near | 13.81u | 439.9m | 457.3m | 439.9m | 117.9m | 1.588a | -109.2a | -288.2a | 428a | 9 |
| near | 14.44u | 443m | 457.3m | 443m | 119.4m | 1.613a | -109.2a | -289.8a | 429.6a | 1 |
| pass | 15.03u | 445.7m | 457.3m | 445.7m | 120.8m | 1.635a | -109.2a | -291.2a | 431a | 1 |
| pass | 15.59u | 448.3m | 457.3m | 448.3m | 122.1m | 1.655a | -109.2a | -292.5a | 432.2a | 1 |
| pass | 16.11u | 450.6m | 457.3m | 450.6m | 123.3m | 1.674a | -109.3a | -293.7a | 433.4a | |
| pass | 16.6u | 452.8m | 457.3m | 452.8m | 124.5m | 1.691a | -109.3a | -294.7a | 434.4a | 1 |
| pass | 17.05u | 454.7m | 457.3m | 454.7m | 125.5m | 1.707a | -109.3a | -295.6a | 435.3a | 1 |
| near | 4.894u | 433.2m | 453.2m | 433.2m | 91.21m | 2.324a | -109.8a | -625.8a | 771.5a | 1 |
| near | 5.25u | 437.1m | 453.2m | 437.1m | 93.06m | 2.345a | -109.8a | -632.1a | 777.1a | 1 |
| near | 5.574u | 440.5m | 453.2m | 440.5m | 94.69m | 2.363a | -109.8a | -637.4a | 781.8a | 1 |
| near | 5.872u | 443.5m | 453.2m | 443.5m | 96.17m | 2.378a | -109.9a | -642a | 785.8a | 2 |
| pass | 6.15u | 446.3m | 453.2m | 446.3m | 97.52m | 2.391a | -109.9a | -646a | 789.4a | 2 |

Simulation results can be saved on CSV file for future editing with other tools like Matlab, Octave, Excel, etc.

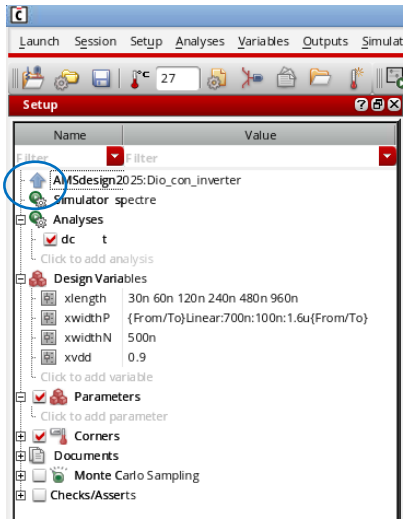
V_VTRIP results can be plotted and the variation of this voltage analyzed for the different transistors sizes combinations. See example below.



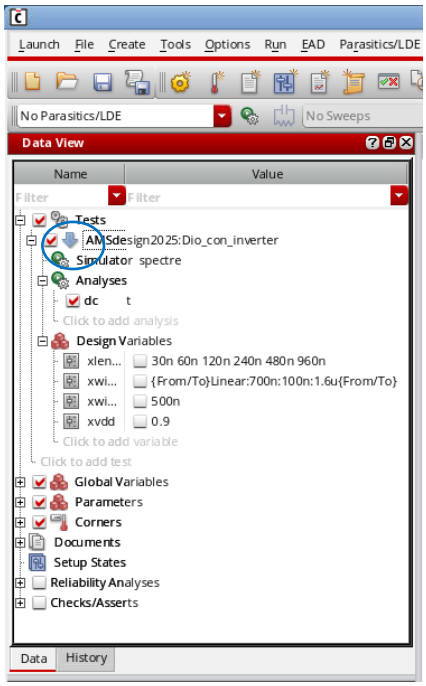

## 4.4. Switch from ADE Explorer to ADE Assembler (and vice versa)

Click on the  to switch from ADE explorer to ADE Assembler (it is possible to return to ADE explorer again with the inverse procedure).

ADE Explorer

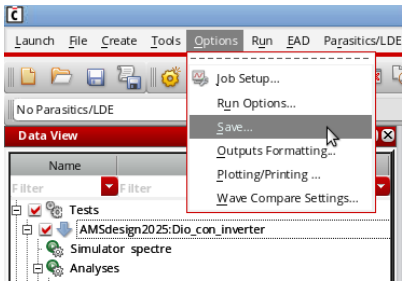


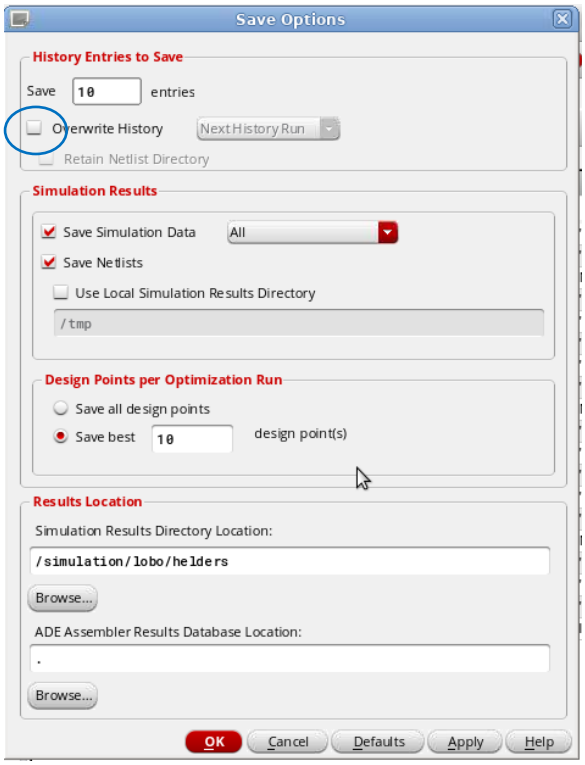

ADE Assembler




ADE Assembler has the possibility to create multiple “Tests”, with different Analyses, Schematics, configurations, etc.

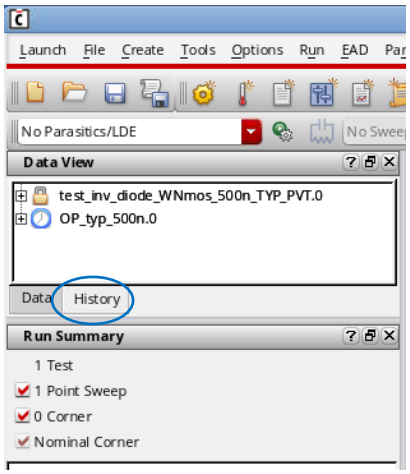
A very useful feature on ADE Assembler is the possibility to easily access the history of the simulations run. To be able to save different names for each simulation access the “Save Options” dialog box and uncheck the “Overwrite History” option, like the example below.




It is also possible to edit the simulation results location path.

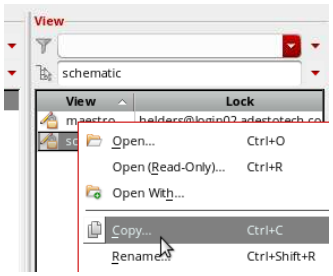
See example below with 3 different simulations on ADE Assembler history dialog box.

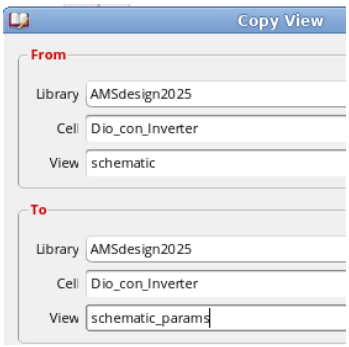


## 4.5. Add a second test to same Maestro on ADE Assembler

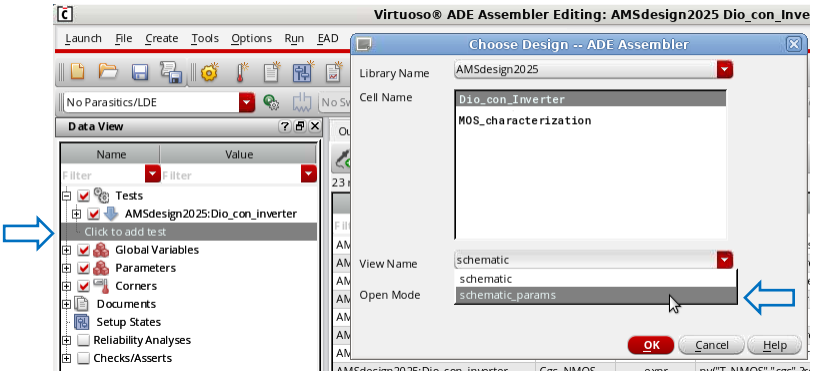
As mentioned above, it is possible to add different tests to the same Maestro Assembler and associate a different schematic.

Copy the current schematic view to a new view and give a different name, see example below.

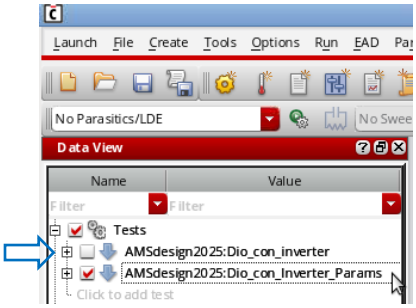


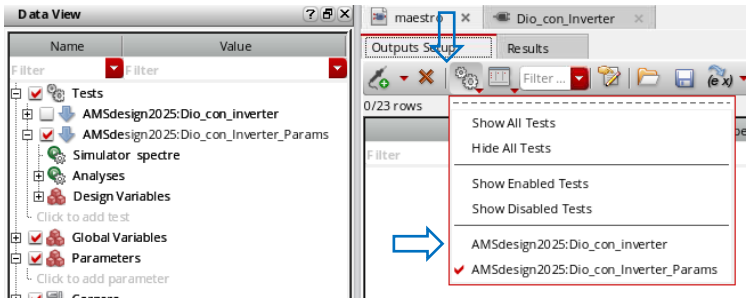

To create a new test setup “Click to add test” and select the current working cell name (“Dio_con_Inverter” on the example above). On the View Name select the new copied version.



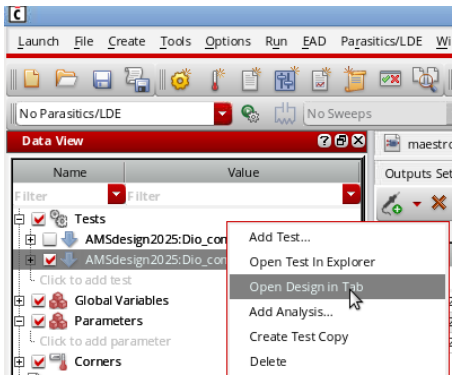

Unselect the first test, so it does not run simultaneously, and give a suitable name to the second test (click twice on the name to edit it). See example below.



To hide the measurements from the first test, uncheck them. See below.

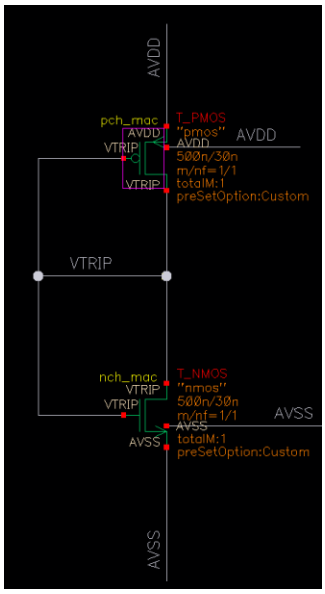



Open the schematic view with design in tab option. See example below.




Confirm the schematic opened is the one you have saved with a different view name (“schematic_params”).

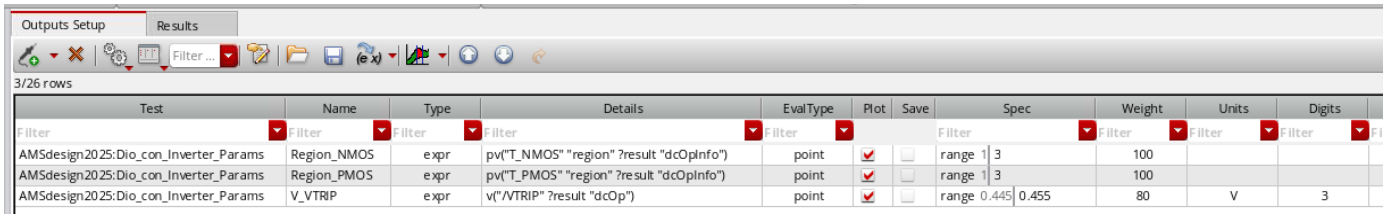
On the schematic, delete the variables on both transistors and add fixed values. See example below.





Run the simulation with nominal conditions (typical process and xvdd=0.9V).

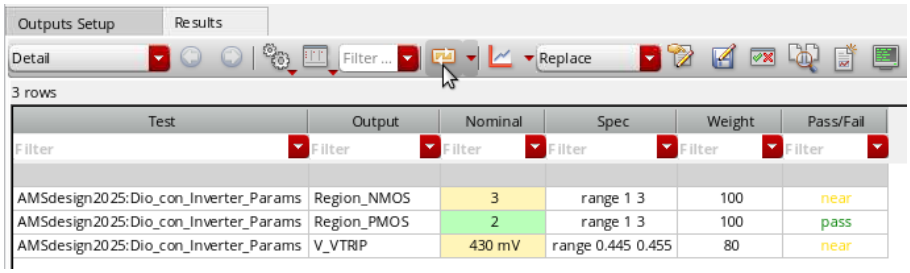
Create the following measurements (if necessary, revisit point 3.6 above on how to add expressions to ADE) and edit the specs column as the example below.




| Test | Name | Type | Details | EvalType | Plot | Save | Spec | Weight | Units | Digits |
|---|---|---|---|---|---|---|---|---|---|---|
| AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | expr | pv("T_NMOS" "region" ?result "dcOpInfo") | point | ✓ | | range 1 3 | 100 | | |
| AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | expr | pv("T_PMOS" "region" ?result "dcOpInfo") | point | ✓ | | range 1 3 | 100 | | |
| AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | expr | v("/VTRIP" ?result "dcOp") | point | ✓ | | range 0.445 0.455 | 80 | V | 3 |

We want the transistors to be in saturation (region=2), so define a specification between 1 and 3.
The “Weight” column will define the importance of the specification.

Refresh the results tab. As can be seen below not all results are compliant with specifications.



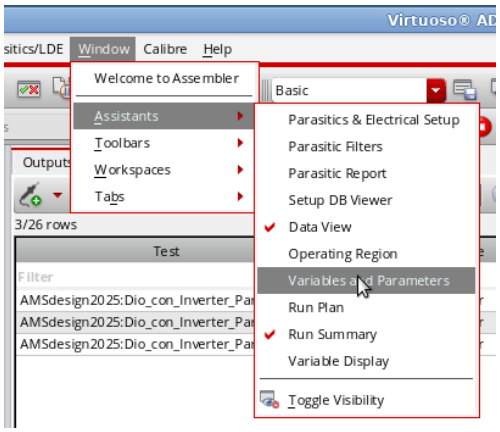

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 3 | range 1 3 | 100 | near |
| AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 | pass |
| AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 430 mV | range 0.445 0.455 | 80 | near |

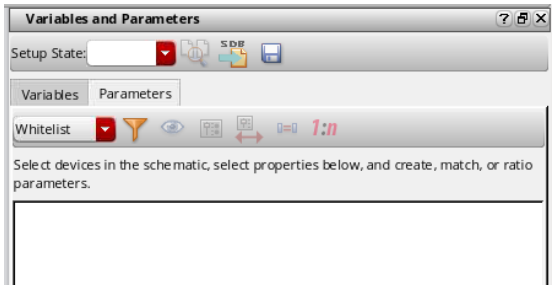
Transistors region meaning:
0 - cut-off
1 - triode
2 - saturation
3 - subthreshold
4 - breakdown

## 4.6. Configure the optimizer to calculate transistors sizes that comply with all specifications

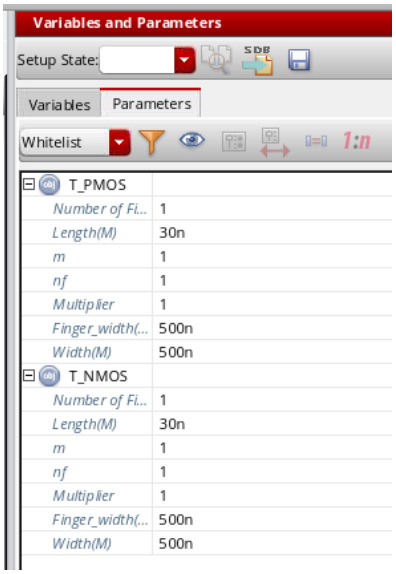
Instead of running a large number of parametric simulations to find the best size for the transistors to match with the VTRIP specification, it is possible to use the Virtuoso optimizer.

To prepare the Maestro for running the optimizer, it is necessary to set initial values. On ADE assembler open the “Variables and Parameters” tab.

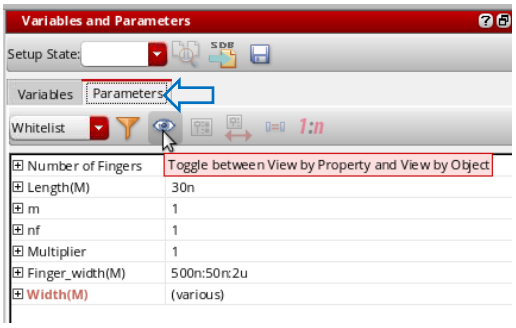


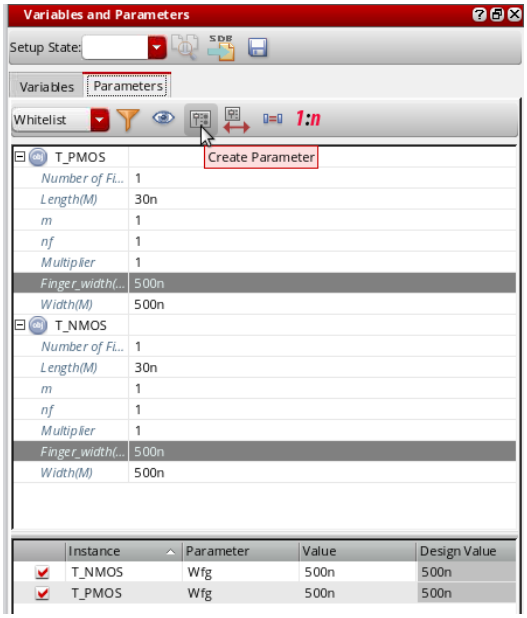
On the schematic editor select the 2 transistors simultaneously and go back to Maestro environment. The transistors parameters should be displayed like the example below.



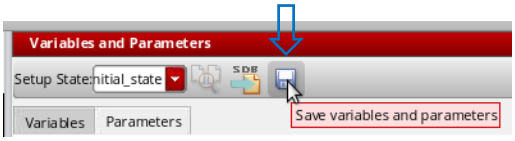

Is possible to toggle between “View by Property” and “View by Object” using the eye tab below.

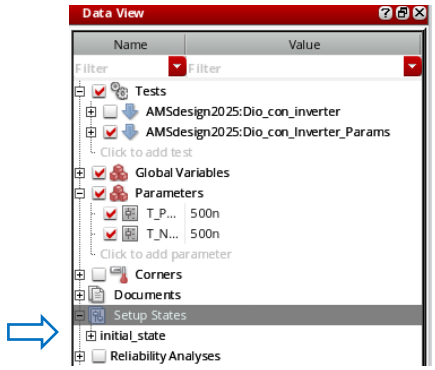



Select both the transistors “Finger_Width(M)” and click on “Create Parameter” icon.

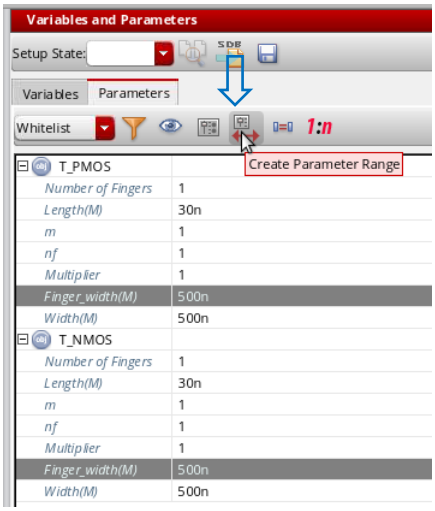


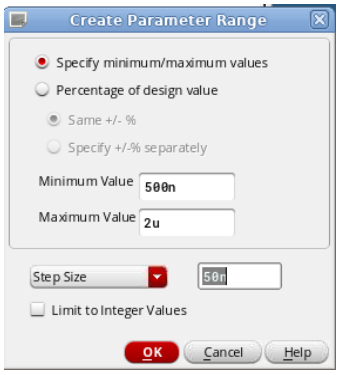
Save the defined parameters as “initial_state” file. Saved state should appear on “Setup States” tab.

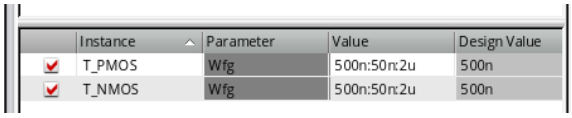


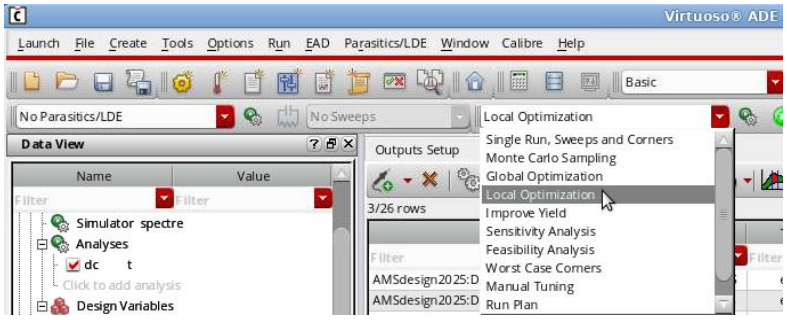

Update the transistors “Finger_Width(M)” value to change from 500nm to 2um in steps of 50nm. See the example below.



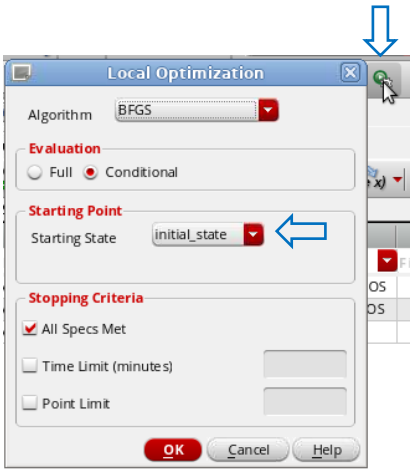




Change the type of simulation to “Local Optimization”. See example below.

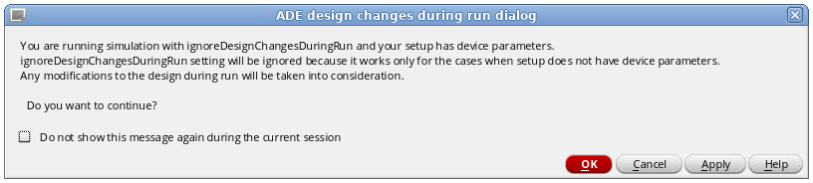


Confirm the “Starting State” on simulation option tab is selected.

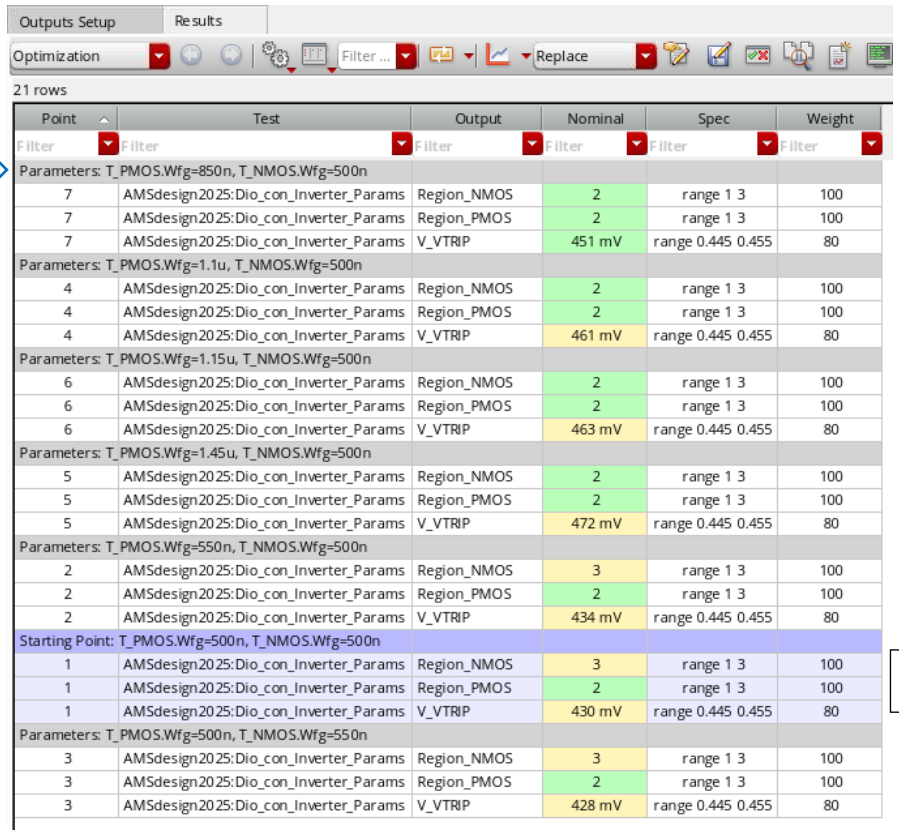



Run the simulation.

If a dialog box like the below appears click Ok, do not change the schematic or Maestro configurations during the optimization simulations process.




The optimization process will start with successive approximations, taking into consideration the specifications and weights given. When all specs are complied, the simulation stops and final sizes are presented.

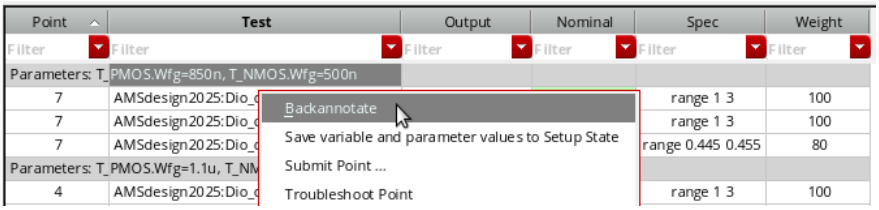


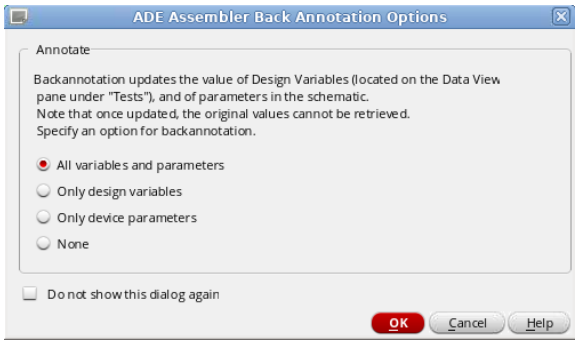

| Point | Test | Output | Nominal | Spec | Weight |
|---|---|---|---|---|---|
| Parameters: T_PMOS.Wfg=850n, T_NMOS.Wfg=500n | | | | | |
| 7 | AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 2 | range 1 3 | 100 |
| 7 | AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 |
| 7 | AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 451 mV | range 0.445 0.455 | 80 |
| Parameters: T_PMOS.Wfg=1.1u, T_NMOS.Wfg=500n | | | | | |
| 4 | AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 2 | range 1 3 | 100 |
| 4 | AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 |
| 4 | AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 461 mV | range 0.445 0.455 | 80 |
| Parameters: T_PMOS.Wfg=1.15u, T_NMOS.Wfg=500n | | | | | |
| 6 | AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 2 | range 1 3 | 100 |
| 6 | AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 |
| 6 | AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 463 mV | range 0.445 0.455 | 80 |
| Parameters: T_PMOS.Wfg=1.45u, T_NMOS.Wfg=500n | | | | | |
| 5 | AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 2 | range 1 3 | 100 |
| 5 | AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 |
| 5 | AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 472 mV | range 0.445 0.455 | 80 |
| Parameters: T_PMOS.Wfg=550n, T_NMOS.Wfg=500n | | | | | |
| 2 | AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 3 | range 1 3 | 100 |
| 2 | AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 |
| 2 | AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 434 mV | range 0.445 0.455 | 80 |
| Starting Point: T_PMOS.Wfg=500n, T_NMOS.Wfg=500n | | | | | |
| 1 | AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 3 | range 1 3 | 100 |
| 1 | AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 |
| 1 | AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 430 mV | range 0.445 0.455 | 80 |
| Parameters: T_PMOS.Wfg=500n, T_NMOS.Wfg=550n | | | | | |
| 3 | AMSdesign2025:Dio_con_Inverter_Params | Region_NMOS | 3 | range 1 3 | 100 |
| 3 | AMSdesign2025:Dio_con_Inverter_Params | Region_PMOS | 2 | range 1 3 | 100 |
| 3 | AMSdesign2025:Dio_con_Inverter_Params | V_VTRIP | 428 mV | range 0.445 0.455 | 80 |

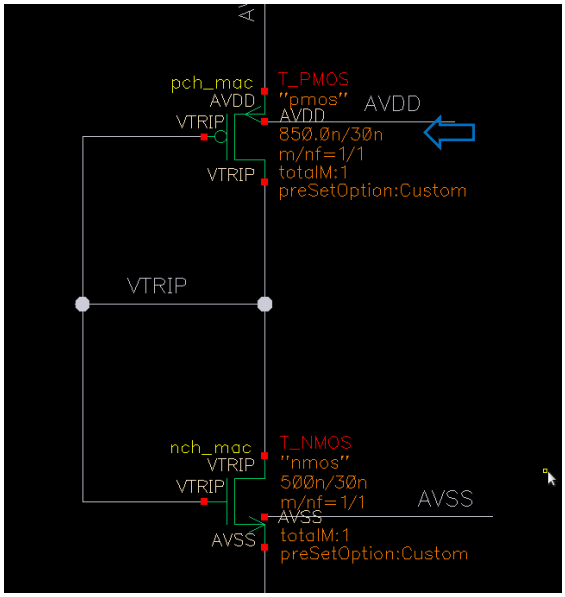
Final results and respective transistors sizes

Initial sizes sim results

It is possible to back annotate the parameters to the schematic.





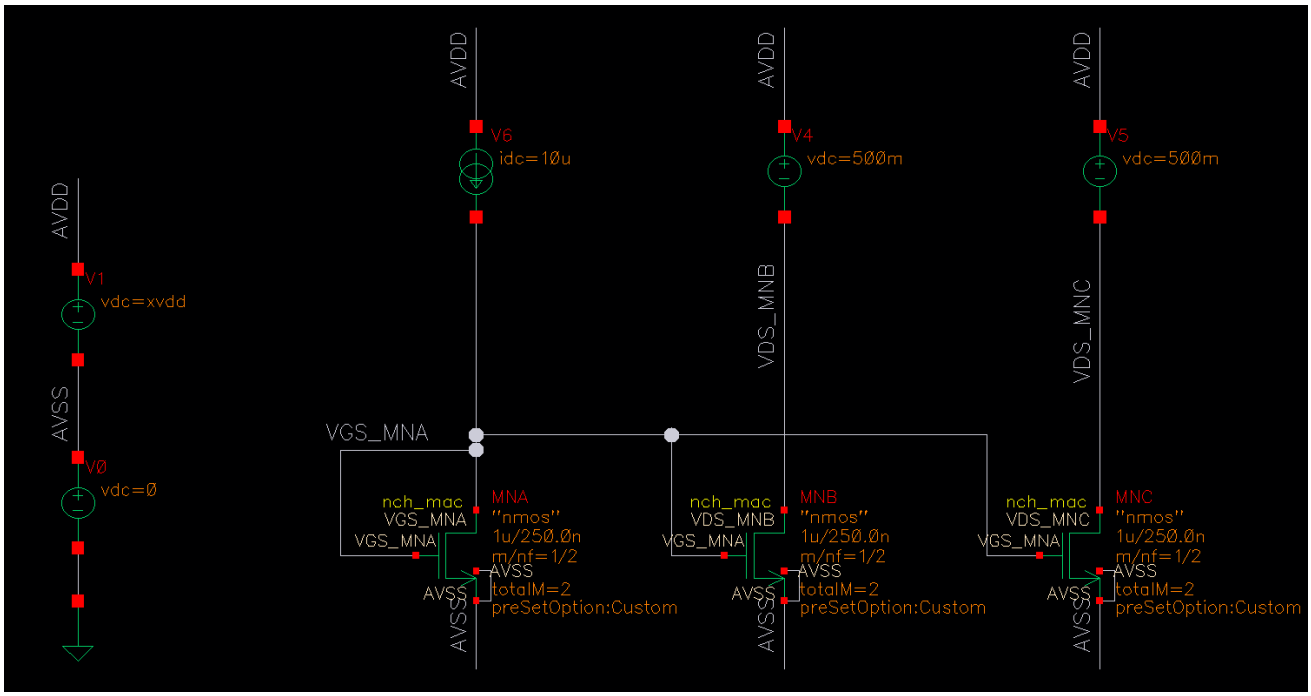
# 5. PVT corners simulations

## 5.1. NMOS current mirror schematic

Copy simple NMOS current mirror schematic from reference library.

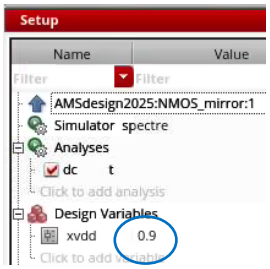
| Library | Cell | View |
|---|---|---|
| MODULE_TECH_PVT_MC | NMOS_mirror | schematic |

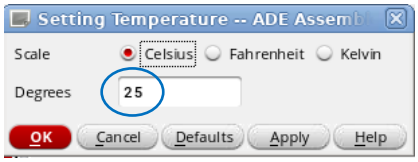
All NMOS have the same size, MNB and MNC have the same VDS voltage. Values have been chosen to set the transistors in saturation region for better current mirroring. An ideal 10uA current is applied to MNA.



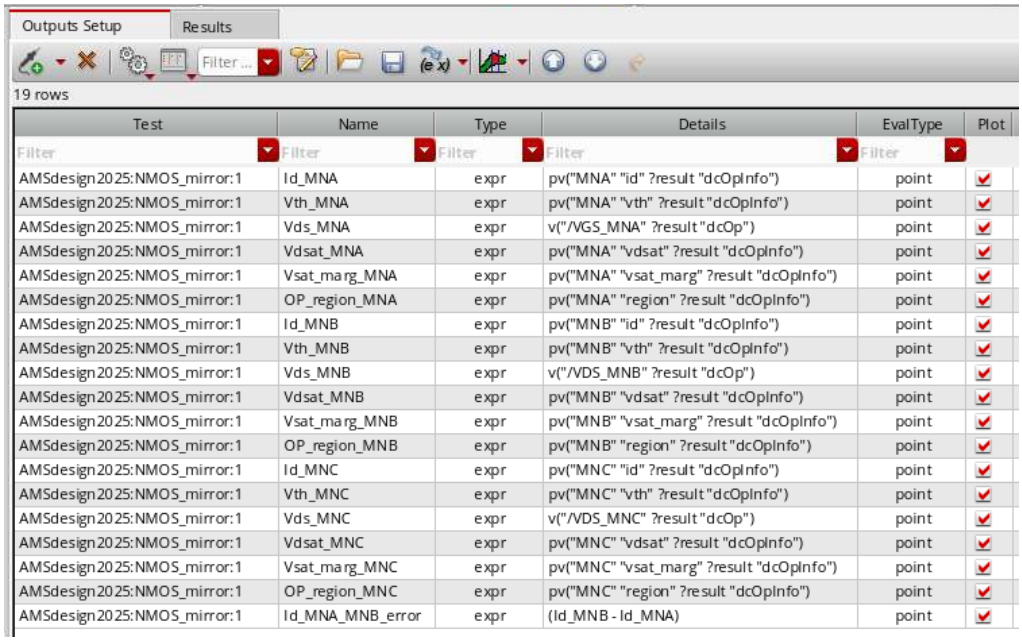

## 5.2. TYP PVT corner simulation

Create a new Maestro ADE Explorer environment.
Edit Models File path (see point 3.5 for more details). Configure the devices models section as "TTTT_RT_CT_BT" (typical Process), supply voltage as 0.9V (typical technology supply value) and temperature as typical 25ºC.



Run the simulation with the above operating conditions and save the following measures to ADE (follow the same steps presented on point 3.6 above).



Outputs Setup | Results

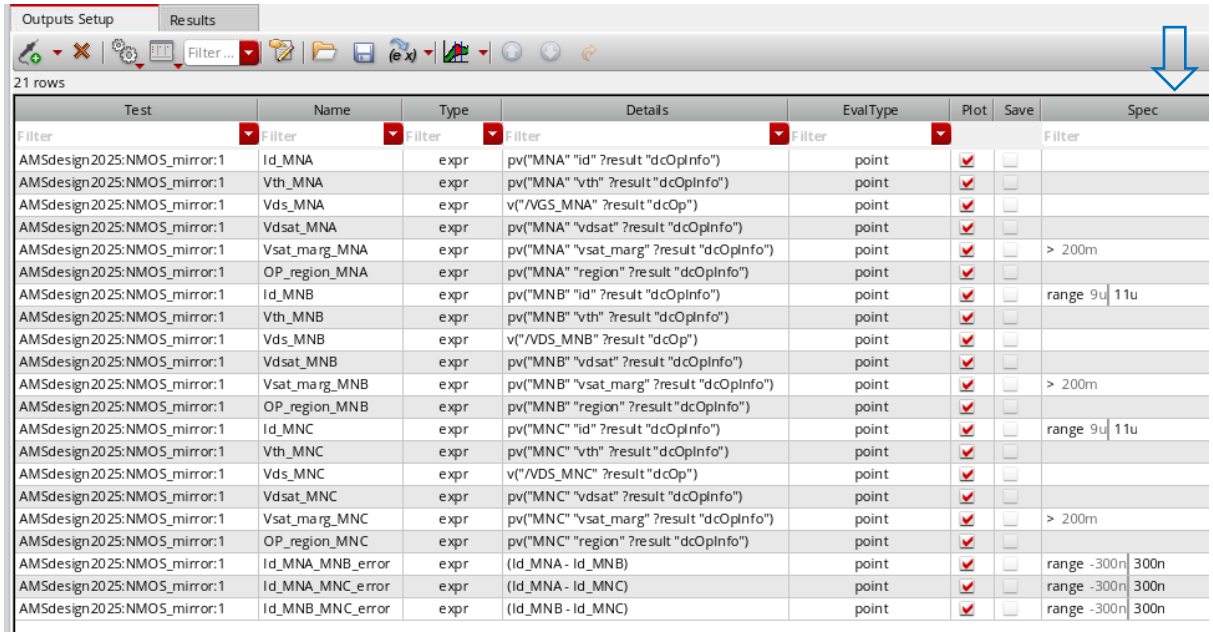
19 rows

| Test | Name | Type | Details | EvalType | Plot |
|---|---|---|---|---|---|
| AMSdesign2025:NMOS_mirror:1 | Id_MNA | expr | pv("MNA" "id" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNA | expr | pv("MNA" "vth" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNA | expr | v("/VGS_MNA" ?result "dcOp") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNA | expr | pv("MNA" "vdsat" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNA | expr | pv("MNA" "vsat_marg" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNA | expr | pv("MNA" "region" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB | expr | pv("MNB" "id" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNB | expr | pv("MNB" "vth" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNB | expr | v("/VDS_MNB" ?result "dcOp") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNB | expr | pv("MNB" "vdsat" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNB | expr | pv("MNB" "vsat_marg" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNB | expr | pv("MNB" "region" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Id_MNC | expr | pv("MNC" "id" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNC | expr | pv("MNC" "vth" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNC | expr | v("/VDS_MNC" ?result "dcOp") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNC | expr | pv("MNC" "vdsat" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNC | expr | pv("MNC" "vsat_marg" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNC | expr | pv("MNC" "region" ?result "dcOpInfo") | point | ☑ |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNB_error | expr | (Id_MNB - Id_MNA) | point | ☑ |

Alternatively, load the following pre-defined measurements file path:
~/IC6_workspace / MODULE_TECH_PVT_MC / outputs_AMSdesign2025_NMOS_mirror_maestro.csv

## 5.3. Define Specifications values (specs) for the measures

One good way to easily evaluate if a measurement is close or even out of specification is to add min/max or range values into ADE and the result will be plotted with a color scheme. See examples below:



Outputs Setup | Results

21 rows

| Test | Name | Type | Details | EvalType | Plot | Save | Spec |
|---|---|---|---|---|---|---|---|
| AMSdesign2025:NMOS_mirror:1 | Id_MNA | expr | pv("MNA" "id" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNA | expr | pv("MNA" "vth" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNA | expr | v("/VGS_MNA" ?result "dcOp") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNA | expr | pv("MNA" "vdsat" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNA | expr | pv("MNA" "vsat_marg" ?result "dcOpInfo") | point | ☑ | ☐ | > 200m |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNA | expr | pv("MNA" "region" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB | expr | pv("MNB" "id" ?result "dcOpInfo") | point | ☑ | ☐ | range 9u 11u |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNB | expr | pv("MNB" "vth" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNB | expr | v("/VDS_MNB" ?result "dcOp") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNB | expr | pv("MNB" "vdsat" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNB | expr | pv("MNB" "vsat_marg" ?result "dcOpInfo") | point | ☑ | ☐ | > 200m |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNB | expr | pv("MNB" "region" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNC | expr | pv("MNC" "id" ?result "dcOpInfo") | point | ☑ | ☐ | range 9u 11u |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNC | expr | pv("MNC" "vth" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNC | expr | v("/VDS_MNC" ?result "dcOp") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNC | expr | pv("MNC" "vdsat" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNC | expr | pv("MNC" "vsat_marg" ?result "dcOpInfo") | point | ☑ | ☐ | > 200m |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNC | expr | pv("MNC" "region" ?result "dcOpInfo") | point | ☑ | ☐ | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNB_error | expr | (Id_MNA - Id_MNB) | point | ☑ | ☐ | range -300n 300n |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNC_error | expr | (Id_MNA - Id_MNC) | point | ☑ | ☐ | range -300n 300n |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB_MNC_error | expr | (Id_MNB - Id_MNC) | point | ☑ | ☐ | range -300n 300n |

## 5.4. Typical corner simulation results

Run the simulation configured with typical operating conditions (TYP PVT). See below an example of results.

Outputs Setup | Results

Detail | Filter ... | Replace

21 rows

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| AMSdesign2025:NMOS_mirror:1 | Id_MNA | 10u | | | |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNA | 463m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNA | 499.6m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNA | 115.6m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNA | 384m | > 200m | | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNA | 2 | | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB | 9.883u | range 9u 11u | | pass |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNB | 463m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNB | 400m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNB | 115.6m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNB | 284.4m | > 200m | | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNB | 2 | | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNC | 9.883u | range 9u 11u | | pass |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNC | 463m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNC | 400m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNC | 115.6m | | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNC | 284.4m | > 200m | | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNC | 2 | | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNB_error | 117.3n | range -300n 300n | | pass |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNC_error | 117.3n | range -300n 300n | | pass |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB_MNC_error | 0 | range -300n 300n | | pass |

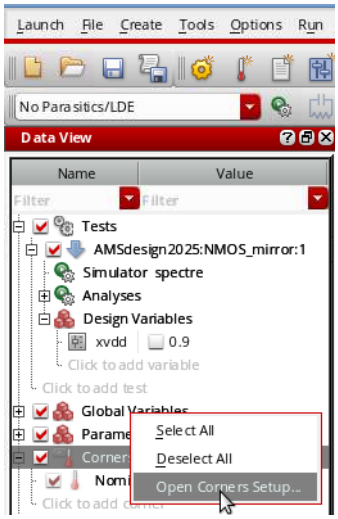
Transistors MNB and MNC have the same operating conditions, as expected, they have equal drain currents. Although, they are different from MNA due to different Vds voltages.

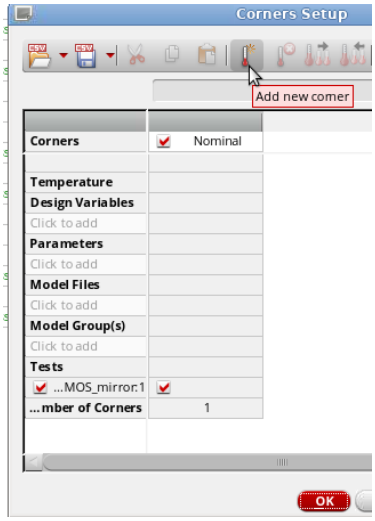
All transistors are on saturation region with good saturation margins.

Transistors region meaning:
0 - cut-off
1 - triode
2 - saturation
3 - subthreshold
4 - breakdown

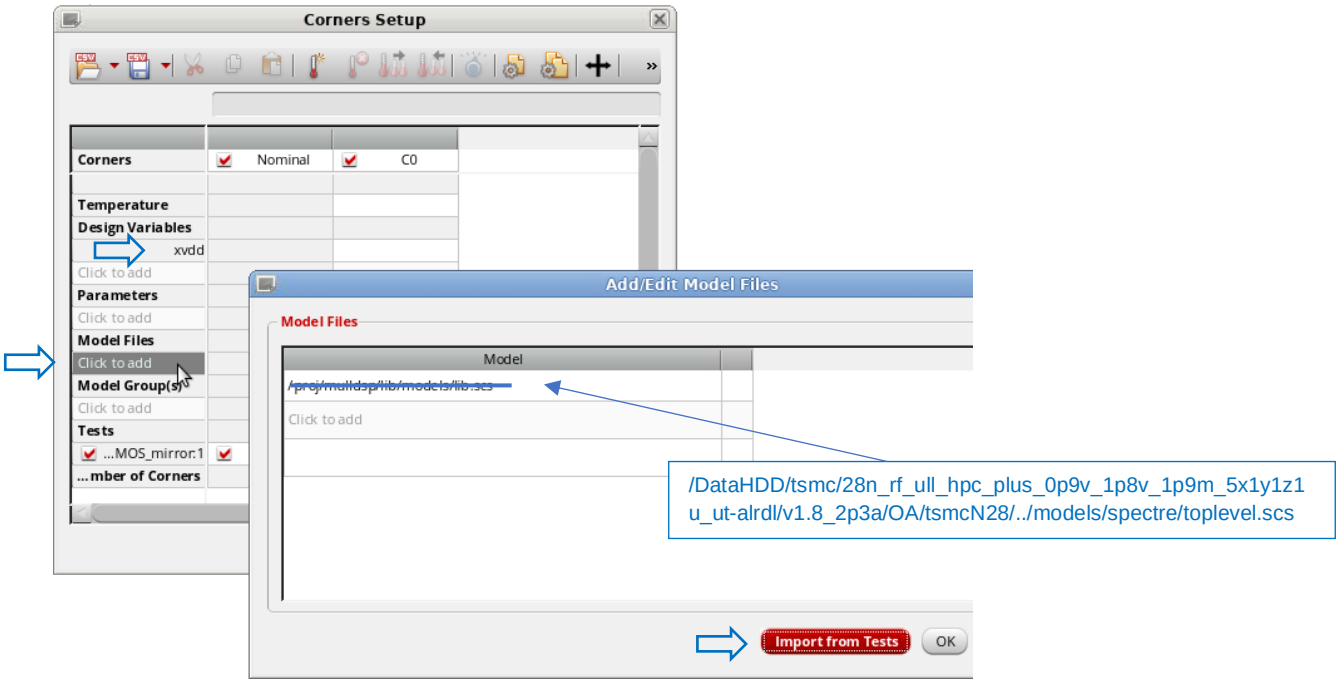
## 5.5. Define corner variations

To add PVT corner variations, launch the “Open Corners Setup…” dialog box and add a new corner.

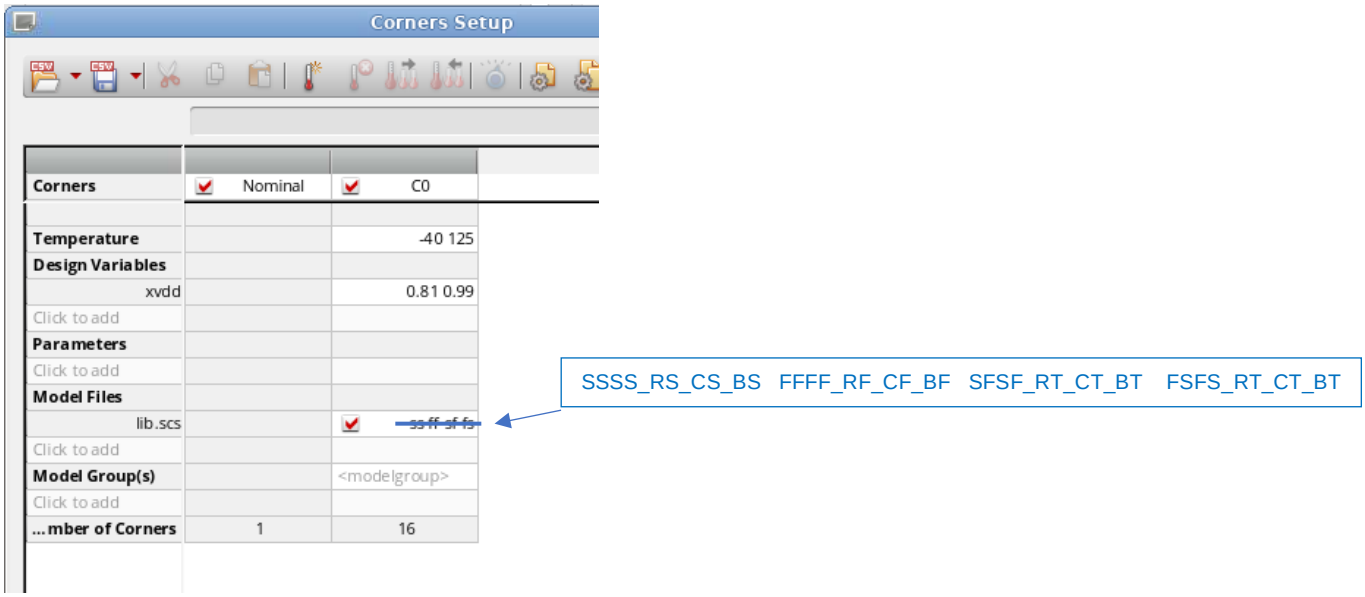



On the new corner add the “Design Variables” and “Model Files” paths, as the example below:



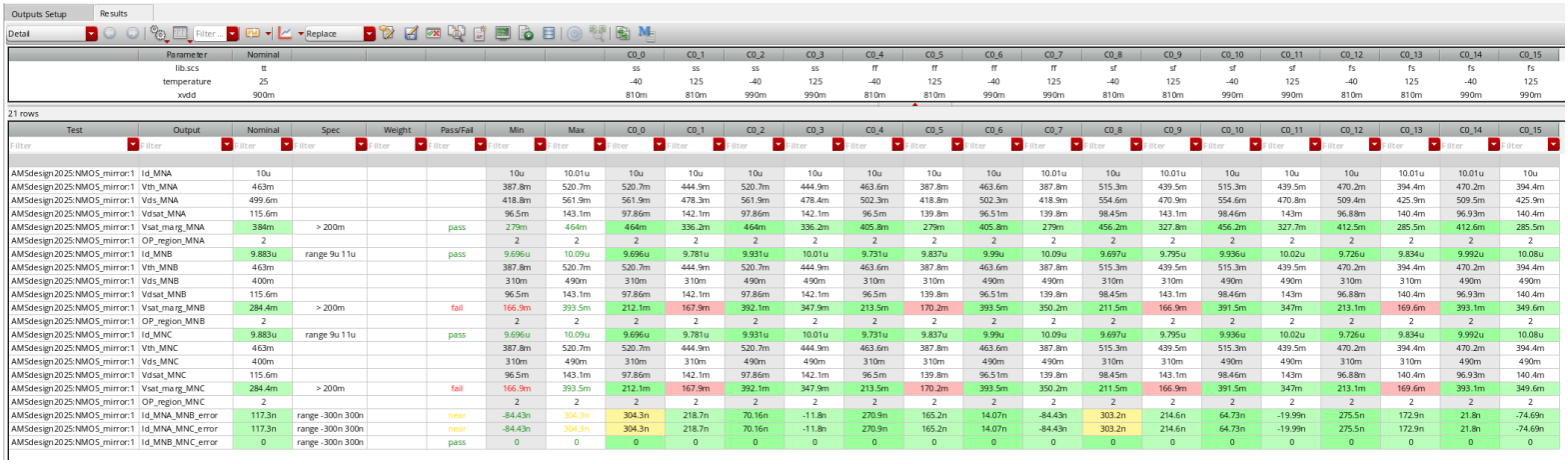

Add the Process, Voltage and Temperature corner values to be simulated.




Please note, the ADE will cross all values added independently and run a simulation for each possible combination. The total number of simulations is added to the bottom of corners setup dialog box.

## 5.6. Corners simulations results

Run the PVT corners simulations. See example of results below:



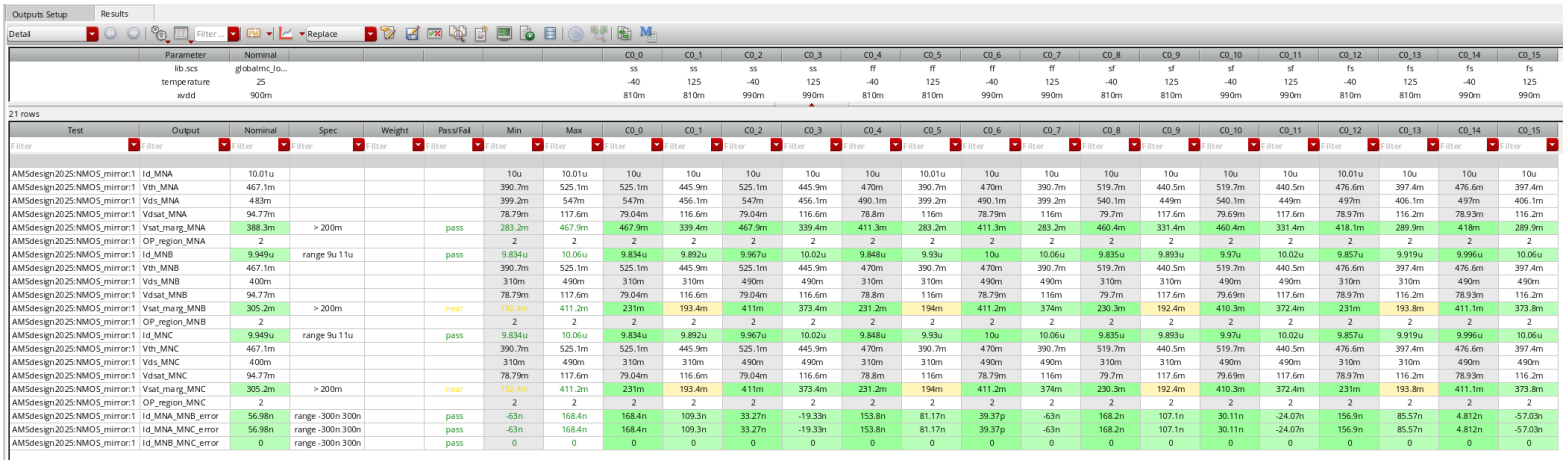
| Parameter | Nominal | C0_0 | C0_1 | C0_2 | C0_3 | C0_4 | C0_5 | C0_6 | C0_7 | C0_8 | C0_9 | C0_10 | C0_11 | C0_12 | C0_13 | C0_14 | C0_15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| lib.scs | tt | ss | ss | ss | ss | ff | ff | ff | ff | sf | sf | sf | sf | fs | fs | fs | fs |
| temperature | 25 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 |
| xvdd | 900m | 810m | 810m | 990m | 990m | 810m | 810m | 990m | 990m | 810m | 810m | 990m | 990m | 810m | 810m | 990m | 990m |

21 rows

| Test | Output | Nominal | Spec | Weight | Pass/Fail | Min | Max | C0_0 | C0_1 | C0_2 | C0_3 | C0_4 | C0_5 | C0_6 | C0_7 | C0_8 | C0_9 | C0_10 | C0_11 | C0_12 | C0_13 | C0_14 | C0_15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMSdesign20251:NMOS_mirror:1 | Id_MNA | 10u | | | | 10u | 10.01u | 10u | 10u | 10u | 10u | 10u | 10u | 10u | 10.01u | 10u | 10.01u | 10u | 10u | 10u | 10.01u | 10.01u | 10u |
| AMSdesign20251:NMOS_mirror:1 | Vth_MNA | 463m | | | | 387.8m | 520.7m | 520.7m | 444.9m | 520.7m | 444.9m | 463.6m | 387.8m | 463.6m | 387.8m | 515.3m | 439.5m | 515.3m | 439.5m | 470.2m | 394.4m | 470.2m | 394.4m |
| AMSdesign20251:NMOS_mirror:1 | Vds_MNA | 499.6m | | | | 418.8m | 561.9m | 561.9m | 478.3m | 561.9m | 478.4m | 502.3m | 418.8m | 502.3m | 418.9m | 554.6m | 470.9m | 554.6m | 470.8m | 509.4m | 425.9m | 509.5m | 425.9m |
| AMSdesign20251:NMOS_mirror:1 | Vdsat_MNA | 115.6m | | | | 96.5m | 143.1m | 97.86m | 142.1m | 97.86m | 142.1m | 96.5m | 139.8m | 96.51m | 139.8m | 98.45m | 143.1m | 98.46m | 143m | 96.88m | 140.4m | 96.93m | 140.4m |
| AMSdesign20251:NMOS_mirror:1 | Vsat_marg_MNA | 384m | > 200m | | pass | 279m | 464m | 464m | 336.2m | 464m | 336.2m | 405.8m | 279m | 405.8m | 279m | 456.2m | 327.8m | 456.2m | 327.7m | 412.5m | 285.5m | 412.6m | 285.5m |
| AMSdesign20251:NMOS_mirror:1 | OP_region_MNA | 2 | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMSdesign20251:NMOS_mirror:1 | Id_MNB | 9.883u | range 9u 11u | | pass | 9.696u | 10.09u | 9.696u | 9.781u | 9.931u | 10.01u | 9.731u | 9.837u | 9.99u | 10.09u | 9.697u | 9.795u | 9.936u | 10.02u | 9.726u | 9.834u | 9.992u | 10.08u |
| AMSdesign20251:NMOS_mirror:1 | Vth_MNB | 463m | | | | 387.8m | 520.7m | 520.7m | 444.9m | 520.7m | 444.9m | 463.6m | 387.8m | 463.6m | 387.8m | 515.3m | 439.5m | 515.3m | 439.5m | 470.2m | 394.4m | 470.2m | 394.4m |
| AMSdesign20251:NMOS_mirror:1 | Vds_MNB | 400m | | | | 310m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m |
| AMSdesign20251:NMOS_mirror:1 | Vdsat_MNB | 115.6m | | | | 96.5m | 143.1m | 97.86m | 142.1m | 97.86m | 142.1m | 96.5m | 139.8m | 96.51m | 139.8m | 98.45m | 143.1m | 98.46m | 143m | 96.88m | 140.4m | 96.93m | 140.4m |
| AMSdesign20251:NMOS_mirror:1 | Vsat_marg_MNB | 284.4m | > 200m | | fail | 166.9m | 393.5m | 212.1m | 167.9m | 392.1m | 347.9m | 213.5m | 170.2m | 393.5m | 350.2m | 211.5m | 166.9m | 391.5m | 347m | 213.1m | 169.6m | 393.1m | 349.6m |
| AMSdesign20251:NMOS_mirror:1 | OP_region_MNB | 2 | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMSdesign20251:NMOS_mirror:1 | Id_MNC | 9.883u | range 9u 11u | | pass | 9.696u | 10.09u | 9.696u | 9.781u | 9.931u | 10.01u | 9.731u | 9.837u | 9.99u | 10.09u | 9.697u | 9.795u | 9.936u | 10.02u | 9.726u | 9.834u | 9.992u | 10.08u |
| AMSdesign20251:NMOS_mirror:1 | Vth_MNC | 463m | | | | 387.8m | 520.7m | 520.7m | 444.9m | 520.7m | 444.9m | 463.6m | 387.8m | 463.6m | 387.8m | 515.3m | 439.5m | 515.3m | 439.5m | 470.2m | 394.4m | 470.2m | 394.4m |
| AMSdesign20251:NMOS_mirror:1 | Vds_MNC | 400m | | | | 310m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m |
| AMSdesign20251:NMOS_mirror:1 | Vdsat_MNC | 115.6m | | | | 96.5m | 143.1m | 97.86m | 142.1m | 97.86m | 142.1m | 96.5m | 139.8m | 96.51m | 139.8m | 98.45m | 143.1m | 98.46m | 143m | 96.88m | 140.4m | 96.93m | 140.4m |
| AMSdesign20251:NMOS_mirror:1 | Vsat_marg_MNC | 284.4m | > 200m | | fail | 166.9m | 393.5m | 212.1m | 167.9m | 392.1m | 347.9m | 213.5m | 170.2m | 393.5m | 350.2m | 211.5m | 166.9m | 391.5m | 347m | 213.1m | 169.6m | 393.1m | 349.6m |
| AMSdesign20251:NMOS_mirror:1 | OP_region_MNC | 2 | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMSdesign20251:NMOS_mirror:1 | Id_MNA_MNB_error | 117.3n | range -300n 300n | | near | -84.43n | 304.3n | 304.3n | 218.7n | 70.16n | -11.8n | 270.9n | 165.2n | 14.07n | -84.43n | 303.2n | 214.6n | 64.73n | -19.99n | 275.5n | 172.9n | 21.8n | -74.69n |
| AMSdesign20251:NMOS_mirror:1 | Id_MNA_MNC_error | 117.3n | range -300n 300n | | near | -84.43n | 304.3n | 304.3n | 218.7n | 70.16n | -11.8n | 270.9n | 165.2n | 14.07n | -84.43n | 303.2n | 214.6n | 64.73n | -19.99n | 275.5n | 172.9n | 21.8n | -74.69n |
| AMSdesign20251:NMOS_mirror:1 | Id_MNB_MNC_error | 0 | range -300n 300n | | pass | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

As can be seen from the simulations results, some of the measurements do not pass all the specifications on all corner conditions. At this point you can edit the transistors' sizes to improve the circuits' performance and try to comply with all the specifications. Or, if specifications are extremely hard to comply with, new architectures can be tested.

For example, increase the number of fingers (nf) of all transistors from 2 to 6 and increase the length (L) of all transistors from 250nm to 500nm. See example below of simulation results for increased transistors sizes.



| Parameter | Nominal | C0_0 | C0_1 | C0_2 | C0_3 | C0_4 | C0_5 | C0_6 | C0_7 | C0_8 | C0_9 | C0_10 | C0_11 | C0_12 | C0_13 | C0_14 | C0_15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| lib.scs | globalmc_lo... | ss | ss | ss | ss | ff | ff | ff | ff | sf | sf | sf | sf | fs | fs | fs | fs |
| temperature | 25 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 | -40 | 125 |
| xvdd | 900m | 810m | 810m | 990m | 990m | 810m | 810m | 990m | 990m | 810m | 810m | 990m | 990m | 810m | 810m | 990m | 990m |

21 rows

| Test | Output | Nominal | Spec | Weight | Pass/Fail | Min | Max | C0_0 | C0_1 | C0_2 | C0_3 | C0_4 | C0_5 | C0_6 | C0_7 | C0_8 | C0_9 | C0_10 | C0_11 | C0_12 | C0_13 | C0_14 | C0_15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMSdesign20251:NMOS_mirror:1 | Id_MNA | 10.01u | | | | 10u | 10.01u | 10u | 10u | 10u | 10u | 10u | 10.01u | 10u | 10u | 10u | 10u | 10u | 10u | 10.01u | 10u | 10u | 10u |
| AMSdesign20251:NMOS_mirror:1 | Vth_MNA | 467.1m | | | | 390.7m | 525.1m | 525.1m | 445.9m | 525.1m | 445.9m | 470m | 390.7m | 470m | 390.7m | 519.7m | 440.5m | 519.7m | 440.5m | 476.6m | 397.4m | 476.6m | 397.4m |
| AMSdesign20251:NMOS_mirror:1 | Vds_MNA | 483m | | | | 399.2m | 547m | 547m | 456.1m | 547m | 456.1m | 490.1m | 399.2m | 490.1m | 399.2m | 540.1m | 449m | 540.1m | 449m | 497m | 406.1m | 497m | 406.1m |
| AMSdesign20251:NMOS_mirror:1 | Vdsat_MNA | 94.77m | | | | 78.79m | 117.6m | 79.04m | 116.6m | 79.04m | 116.6m | 78.8m | 116m | 78.79m | 116m | 79.7m | 117.6m | 79.69m | 117.6m | 78.97m | 116.2m | 78.93m | 116.2m |
| AMSdesign20251:NMOS_mirror:1 | Vsat_marg_MNA | 388.3m | > 200m | | pass | 283.2m | 467.9m | 467.9m | 339.4m | 467.9m | 339.4m | 411.3m | 283.2m | 411.3m | 283.2m | 460.4m | 331.4m | 460.4m | 331.4m | 418.1m | 289.9m | 418m | 289.9m |
| AMSdesign20251:NMOS_mirror:1 | OP_region_MNA | 2 | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMSdesign20251:NMOS_mirror:1 | Id_MNB | 9.949u | range 9u 11u | | pass | 9.834u | 10.06u | 9.834u | 9.892u | 9.967u | 10.02u | 9.848u | 9.93u | 10u | 10.06u | 9.835u | 9.893u | 9.97u | 10.02u | 9.857u | 9.919u | 9.996u | 10.06u |
| AMSdesign20251:NMOS_mirror:1 | Vth_MNB | 467.1m | | | | 390.7m | 525.1m | 525.1m | 445.9m | 525.1m | 445.9m | 470m | 390.7m | 470m | 390.7m | 519.7m | 440.5m | 519.7m | 440.5m | 476.6m | 397.4m | 476.6m | 397.4m |
| AMSdesign20251:NMOS_mirror:1 | Vds_MNB | 400m | | | | 310m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m |
| AMSdesign20251:NMOS_mirror:1 | Vdsat_MNB | 94.77m | | | | 78.79m | 117.6m | 79.04m | 116.6m | 79.04m | 116.6m | 78.8m | 116m | 78.79m | 116m | 79.7m | 117.6m | 79.69m | 117.6m | 78.97m | 116.2m | 78.93m | 116.2m |
| AMSdesign20251:NMOS_mirror:1 | Vsat_marg_MNB | 305.2m | > 200m | | near | 192.4m | 411.2m | 231m | 193.4m | 411m | 373.4m | 231.2m | 194m | 411.2m | 374m | 230.3m | 192.4m | 410.3m | 372.4m | 231m | 193.8m | 411.1m | 373.8m |
| AMSdesign20251:NMOS_mirror:1 | OP_region_MNB | 2 | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMSdesign20251:NMOS_mirror:1 | Id_MNC | 9.949u | range 9u 11u | | pass | 9.834u | 10.06u | 9.834u | 9.892u | 9.967u | 10.02u | 9.848u | 9.93u | 10u | 10.06u | 9.835u | 9.893u | 9.97u | 10.02u | 9.857u | 9.919u | 9.996u | 10.06u |
| AMSdesign20251:NMOS_mirror:1 | Vth_MNC | 467.1m | | | | 390.7m | 525.1m | 525.1m | 445.9m | 525.1m | 445.9m | 470m | 390.7m | 470m | 390.7m | 519.7m | 440.5m | 519.7m | 440.5m | 476.6m | 397.4m | 476.6m | 397.4m |
| AMSdesign20251:NMOS_mirror:1 | Vds_MNC | 400m | | | | 310m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m | 310m | 310m | 490m | 490m |
| AMSdesign20251:NMOS_mirror:1 | Vdsat_MNC | 94.77m | | | | 78.79m | 117.6m | 79.04m | 116.6m | 79.04m | 116.6m | 78.8m | 116m | 78.79m | 116m | 79.7m | 117.6m | 79.69m | 117.6m | 78.97m | 116.2m | 78.93m | 116.2m |
| AMSdesign20251:NMOS_mirror:1 | Vsat_marg_MNC | 305.2m | > 200m | | near | 192.4m | 411.2m | 231m | 193.4m | 411m | 373.4m | 231.2m | 194m | 411.2m | 374m | 230.3m | 192.4m | 410.3m | 372.4m | 231m | 193.8m | 411.1m | 373.8m |
| AMSdesign20251:NMOS_mirror:1 | OP_region_MNC | 2 | | | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| AMSdesign20251:NMOS_mirror:1 | Id_MNA_MNB_error | 56.98n | range -300n 300n | | pass | -63n | 168.4n | 168.4n | 109.3n | 33.27n | -19.33n | 153.8n | 81.17n | 39.37p | -63n | 168.2n | 107.1n | 30.11n | -24.07n | 156.9n | 85.57n | 4.812n | -57.03n |
| AMSdesign20251:NMOS_mirror:1 | Id_MNA_MNC_error | 56.98n | range -300n 300n | | pass | -63n | 168.4n | 168.4n | 109.3n | 33.27n | -19.33n | 153.8n | 81.17n | 39.37p | -63n | 168.2n | 107.1n | 30.11n | -24.07n | 156.9n | 85.57n | 4.812n | -57.03n |
| AMSdesign20251:NMOS_mirror:1 | Id_MNB_MNC_error | 0 | range -300n 300n | | pass | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

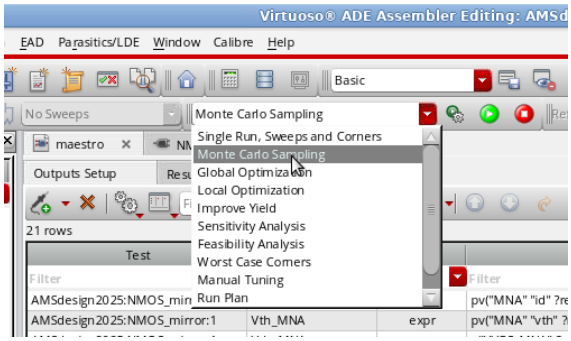
With the adjustments, the saturation margin is much closer to spec, and the mirrored currents errors between MNA and MNB/MNC have been significantly reduced.

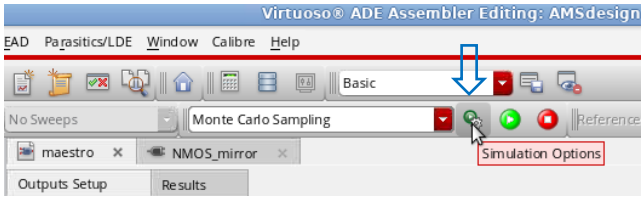
As expected, no error is obtained between Id_MNB and Id_MNC since they share the same operating conditions.

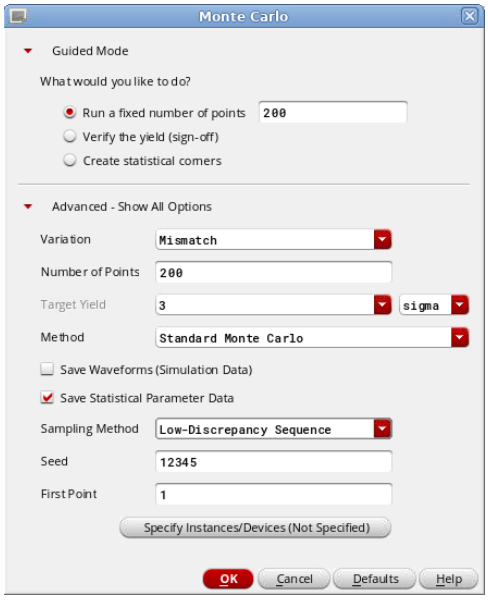
# 6. Monte-Carlo simulations

## 6.1. Configuration of Monte-Carlo simulations

To run simulations of devices process and mismatch variations select the “Monte Carlo Sampling” option on same NMOS current mirror testbench simulated on previous point and open the respective simulations configuration tool.




The number of points will be equivalent to the number of simulations, each one with different variations of each device parameters.

3 types of variations are available:

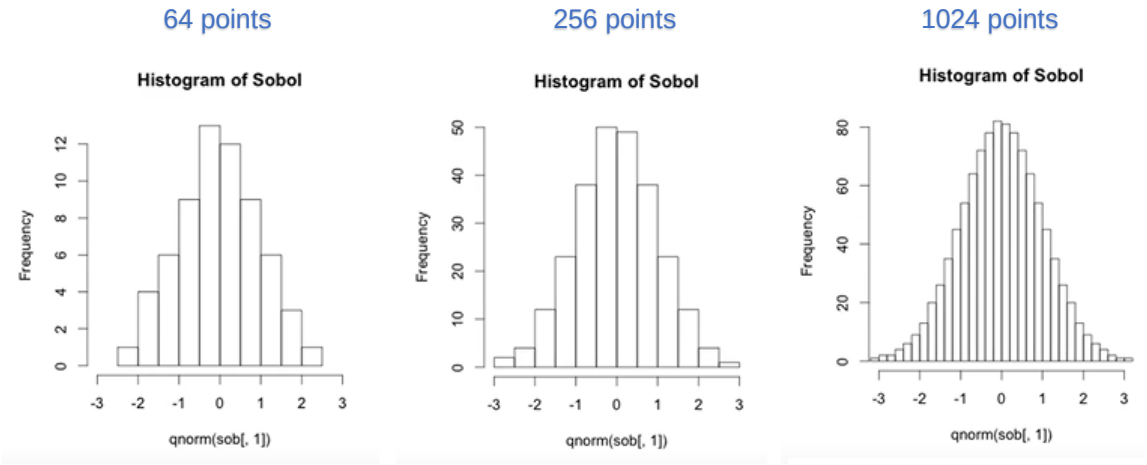
- All (Process + Mismatch)
- Mismatch
- Process

3 Sampling Method are available:

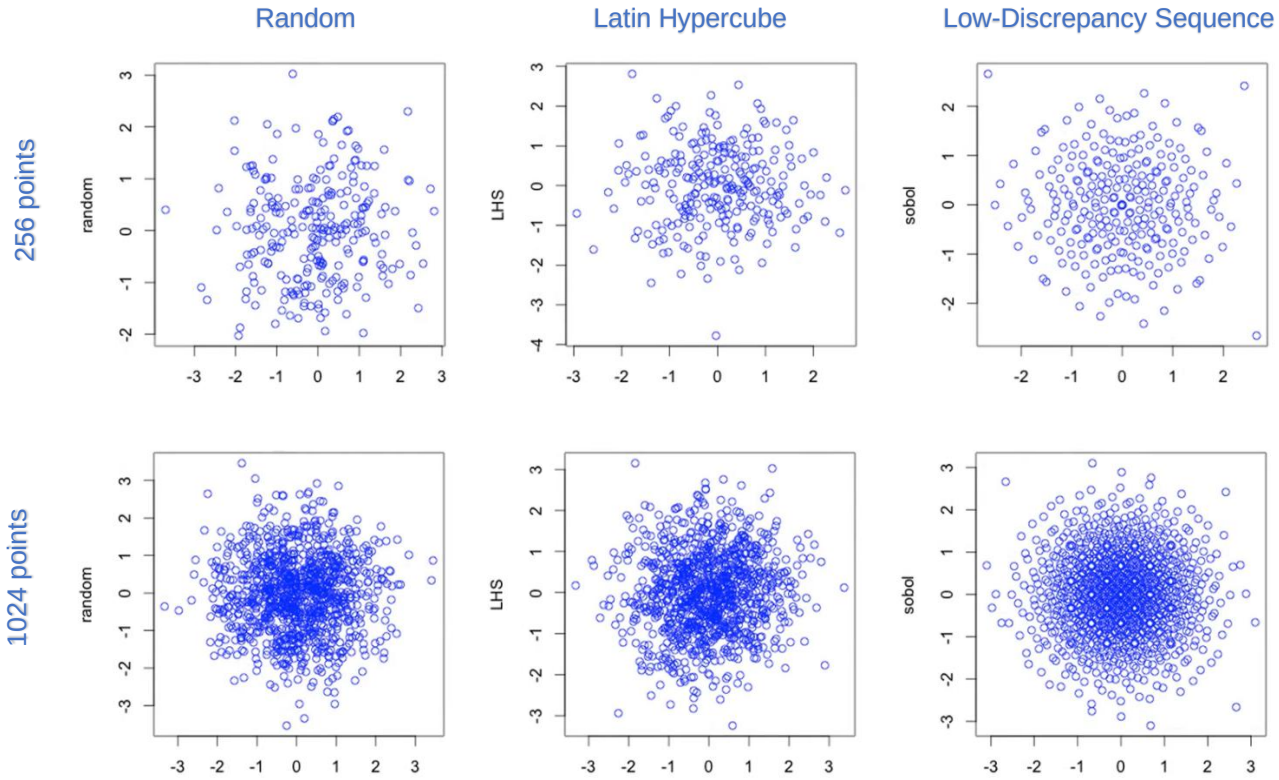
- Random
- Latin Hypercube
- Low-Discrepancy Sequence

Select the “Mismatch” variation, “Low-Discrepancy Sequence” sampling method and 200 points.

The higher the number of points the more accurate the statistical analysis will be. See example below of Gaussian distribution for different number of points (source Cadence Community website):

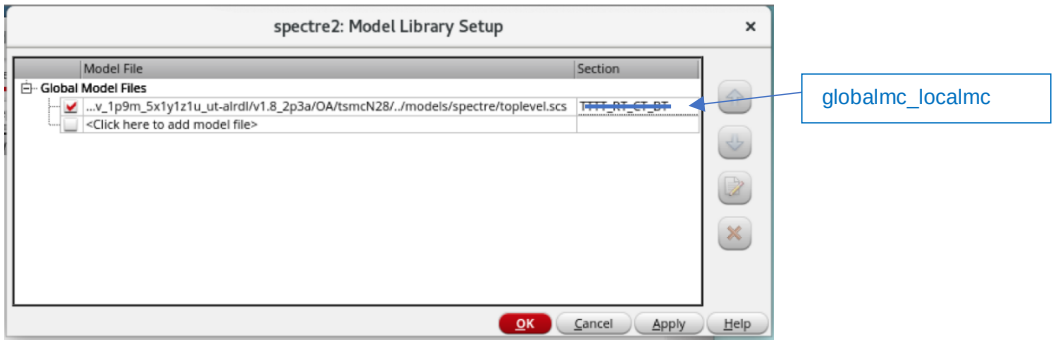



Low-Discrepancy Sequence ensures a better distribution of devices variations across all possible range compared with pure random sequence, which makes it possible to obtain more accurate statistic results with less number of points when compared with pure random sequence. See examples below with the 3 methods for 256 points (source Cadence Community website):

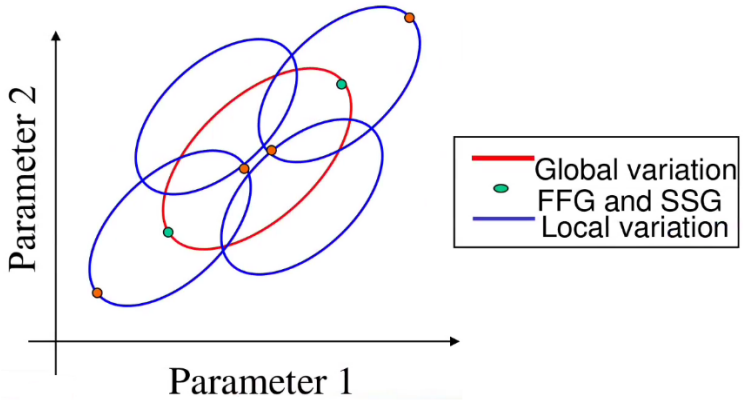


## 6.2. Monte-Carlo Model Libraries files

On “Model Library Setup” dialog box, select the “globalmc_localmc” section. Since only “mismatch” is selected just local mismatch will be run with typical process corner.

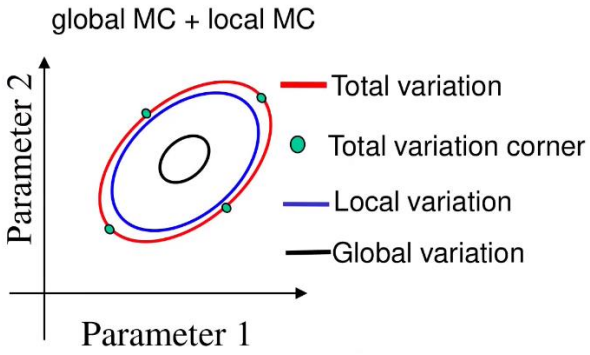



From TSMC “Model Usage Guide” document is possible to understand the statistical variations associated with each section.
On “SSSS_RS_CS_BS”, “FFFF_RF_CF_BF”, “SFSF_RT_CT_BT” and “FSFS_RT_CT_BT” sections, the local mismatch is added on top of each process corner. These options should be used on very sensitive circuits, where matching between branches is essential, like for example Differential Amplifiers, PLL’s, VCO’s, etc.
The plot below is an example of possible statistical variations when “Global Corner + Local Monte-Carlo” sections are selected for simulation.




On “globalmc_localmc” section with Monte-Carlo “All” variations option selected, all devices will have a global variation withing the process statistical distribution plus a local mismatch applied to each device within the mismatch statistical distribution.

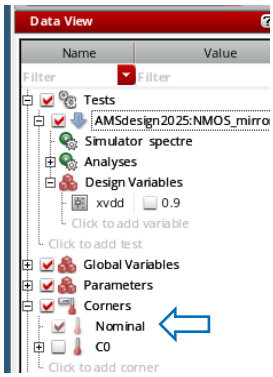
The plot below is an example of possible statistical variations when “Global Monte-Carlo + Local Monte-Carlo” sections are selected for simulation.




$$\sigma_{total}^{2} = \sigma_{global}^{2} + \sigma_{local}^{2}$$

## 6.3. Monte-Carlo Mismatch simulations results

Select just “Nominal” corner and run the simulations.




See example below of measured results summary.
(explore the various formats available of presenting the results)

Outputs Setup | Results

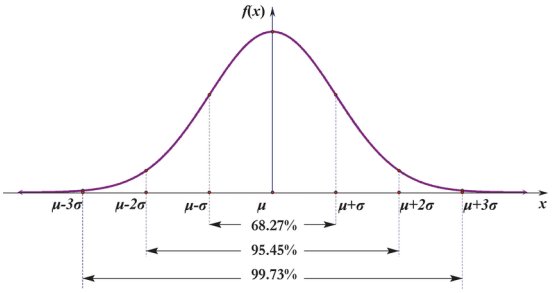
Summary | Replace

| Test | Output | Min | Max | Mean | Median | Std Dev | Spec | Pass/Fail |
|---|---|---|---|---|---|---|---|---|
| AMSdesign2025:NMOS_mirror:1 | Id_MNA | 10u | 10.01u | 10.01u | 10.01u | 1.79n | | |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNA | 462.6m | 470.9m | 467.1m | 467.1m | 1.504m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNA | 478.9m | 486.8m | 483m | 483m | 1.437m | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNA | 94.41m | 95.13m | 94.77m | 94.77m | 130.6u | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNA | 383.9m | 392.1m | 388.2m | 388.3m | 1.473m | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNA | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB | 9.18u | 11.14u | 9.954u | 9.934u | 343.4n | range 9u 11u | near |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNB | 462.4m | 470.9m | 467.1m | 467.1m | 1.516m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNB | 400m | 400m | 400m | 400m | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNB | 92.25m | 98.56m | 94.78m | 94.76m | 1.166m | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNB | 301.4m | 307.8m | 305.2m | 305.2m | 1.166m | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNB | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNC | 8.92u | 11.24u | 9.952u | 9.949u | 346.6n | range 9u 11u | near |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNC | 462.8m | 471.4m | 467.1m | 467m | 1.536m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNC | 400m | 400m | 400m | 400m | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNC | 91.43m | 98.72m | 94.77m | 94.76m | 1.184m | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNC | 301.3m | 308.6m | 305.2m | 305.2m | 1.184m | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNC | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNB_error | -1.125u | 824.6n | 52.91n | 72.34n | 342.1n | range -300n 300n | fail |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNC_error | -1.227u | 1.084u | 54.4n | 56.45n | 345.3n | range -300n 300n | fail |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB_MNC_error | -898.6n | 1.091u | 1.497n | -10.62n | 339n | range -300n 300n | fail |

On point 5, with just PVT corner variations, the bias currents difference between branch B and C (Id_MNB_MNC_error) was 0 for all corners, because all
devices have been affected by the same conditions (global variations). The mismatch between the devices that happens in real silicon (local variations) was not considered.
With the addition of mismatch, even with typical PVT conditions, there will be differences in branches B and C currents

For accurate systems the 3σ is used as an accepted variation of a measured value, it means more than 99% of the samples will be withing this range value.

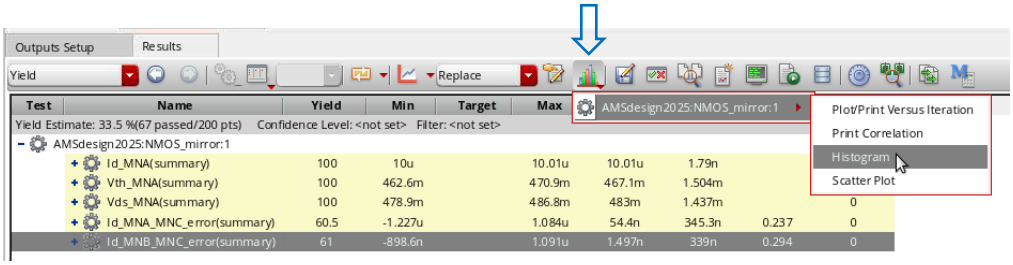
On ADE, we have access to just 1σ variation results (Std Dev). To simplify the calculation of the 3σ usually the 1σ, is multiplied by 3.



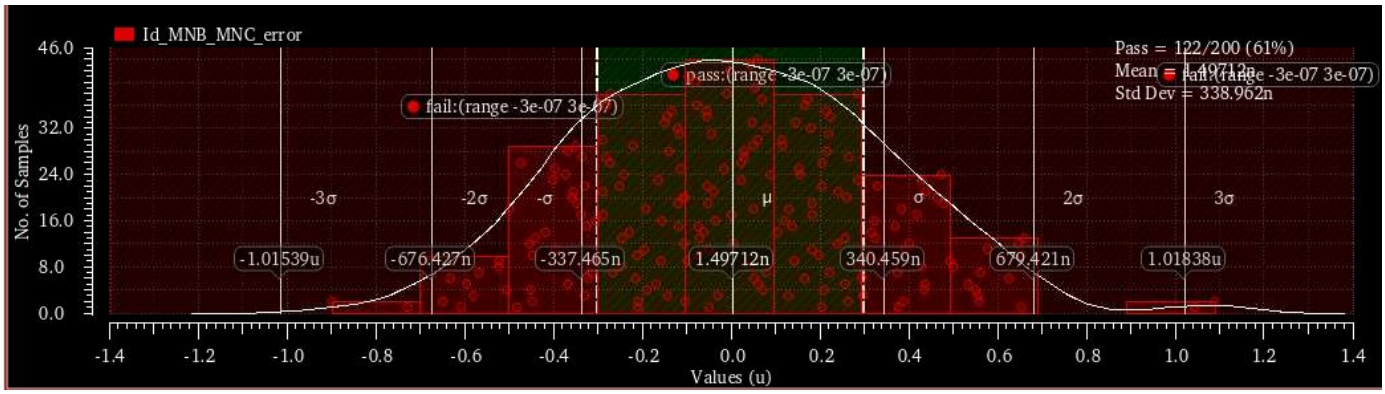

(Source: www.researchgate.net/)

Looking into the Monte-Carlo results, the difference between the drain currents of MNB and MNC
(Id_MNB_MNC_error) has a Std Dev (σ) of 339nA and a mean (μ) of 1.497n. Statistically this means that 99.73% of the cases will be within the interval [μ - 3σ ; μ + 3σ] = [-1.016uA ; 1.018uA].
Computing this error in percentage referring to the 10uA of the mirror we got [-10.16% ; 10.18%] variation between these two currents, which is higher than ±10%.

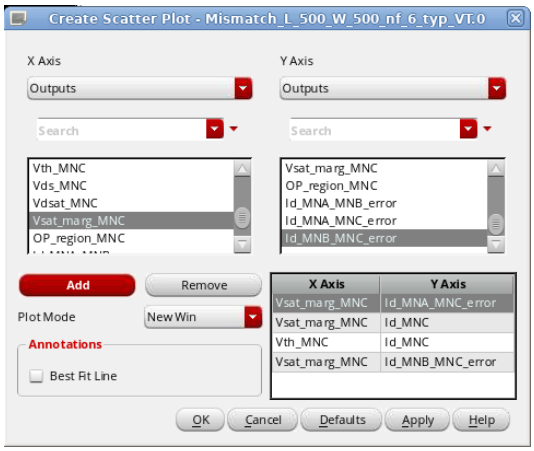
Results can also plot in “Histogram” or “Scatter Plot“ formats.

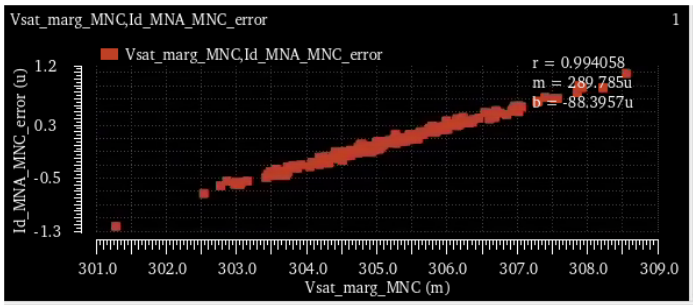


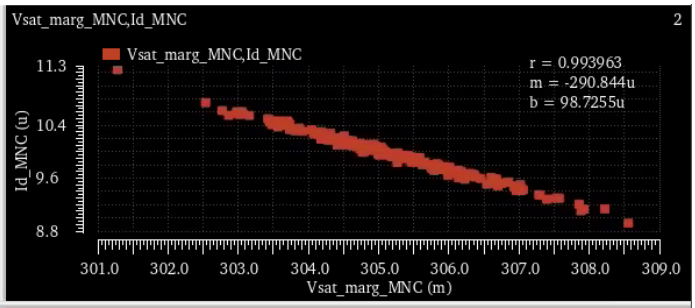

See example of histogram plot below for drain current difference error between transistors MNB and MNC.

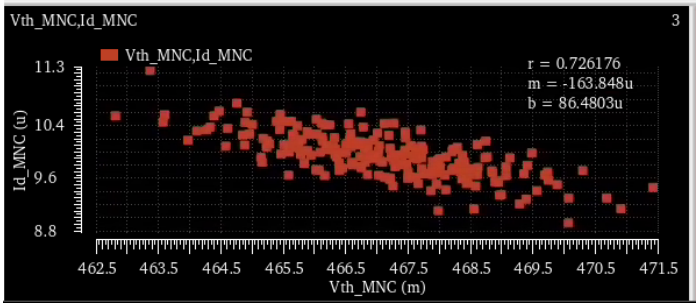


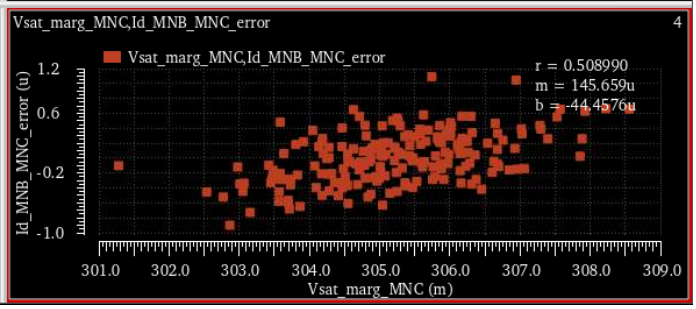
The “Scatter Plot” has the possibility to choose the two axis, see examples below.



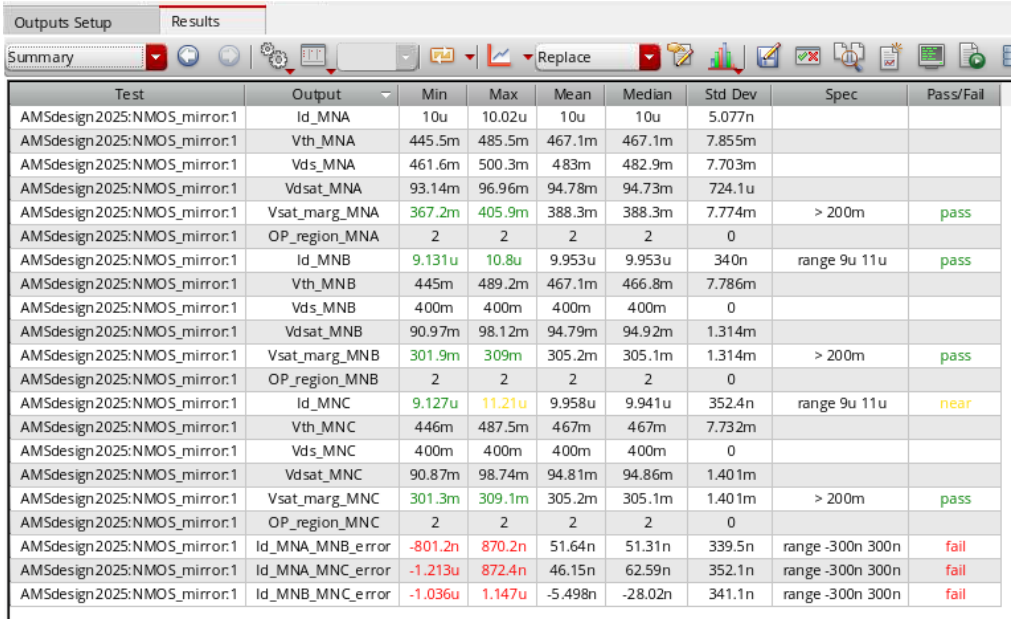



## 6.4. Monte-Carlo Process + Mismatch simulations results

Change the Monte-Carlo variation method from “Mismatch” to “All” (Process + Mismatch) and re-run the simulation. See below example of measured results.




| Test | Output | Min | Max | Mean | Median | Std Dev | Spec | Pass/Fail |
|---|---|---|---|---|---|---|---|---|
| AMSdesign2025:NMOS_mirror:1 | Id_MNA | 10u | 10.02u | 10u | 10u | 5.077n | | |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNA | 445.5m | 485.5m | 467.1m | 467.1m | 7.855m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNA | 461.6m | 500.3m | 483m | 482.9m | 7.703m | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNA | 93.14m | 96.96m | 94.78m | 94.73m | 724.1u | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNA | 367.2m | 405.9m | 388.3m | 388.3m | 7.774m | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNA | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB | 9.131u | 10.8u | 9.953u | 9.953u | 340n | range 9u 11u | pass |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNB | 445m | 489.2m | 467.1m | 466.8m | 7.786m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNB | 400m | 400m | 400m | 400m | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNB | 90.97m | 98.12m | 94.79m | 94.92m | 1.314m | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNB | 301.9m | 309m | 305.2m | 305.1m | 1.314m | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNB | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNC | 9.127u | 11.21u | 9.958u | 9.941u | 352.4n | range 9u 11u | near |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNC | 446m | 487.5m | 467m | 467m | 7.732m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNC | 400m | 400m | 400m | 400m | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNC | 90.87m | 98.74m | 94.81m | 94.86m | 1.401m | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNC | 301.3m | 309.1m | 305.2m | 305.1m | 1.401m | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNC | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNB_error | -801.2n | 870.2n | 51.64n | 51.31n | 339.5n | range -300n 300n | fail |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNC_error | -1.213u | 872.4n | 46.15n | 62.59n | 352.1n | range -300n 300n | fail |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB_MNC_error | -1.036u | 1.147u | -5.498n | -28.02n | 341.1n | range -300n 300n | fail |

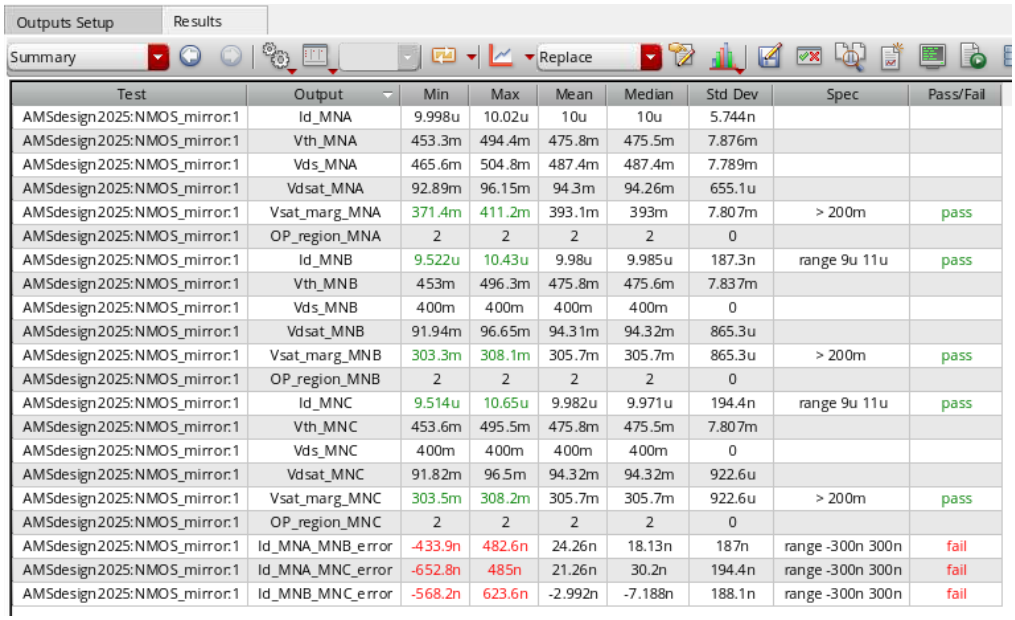
Compare the results with the ones having just mismatch variation. What could we conclude?

- The statistical results are not very different.
- This tells us the mismatch is the dominant factor for the current mirroring error A to B and A to C.
- The mismatch is the only factor affecting the difference between currents in branch B and C.
- This was expected, since we have seen that stand-alone PVT variations were not causing any difference between branch B and branch C currents, as the global variations affect similarly branch B and C paired devices.

Monte-Carlo devices parameters variations have a direct relation with the size of the devices. Higher sizes will exhibit lower variations.
To verify the above sentence, try to increase the size of the transistors by 2x. Please note, to maintain the same operating point, the devices need to maintain the same Width/Length rations.

See example below of measured results summary for bigger devices.

Although the errors between the mirrored currents have not reached the specs, they were significantly reduced with the increase of devices sizes.

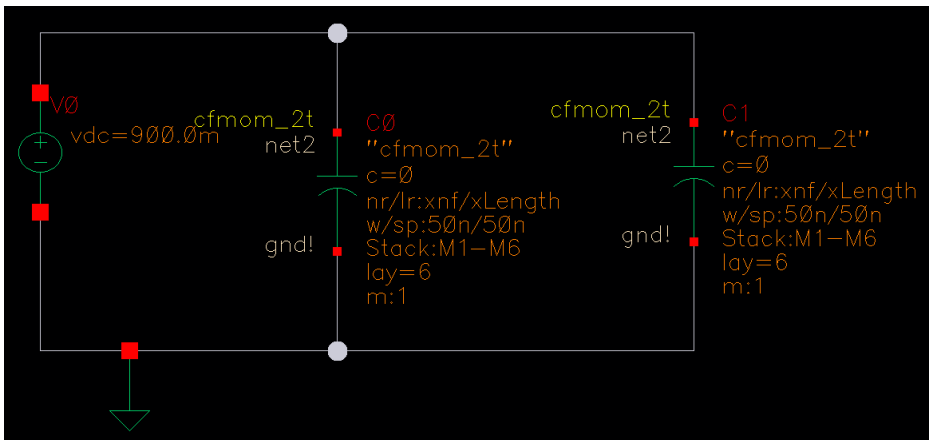


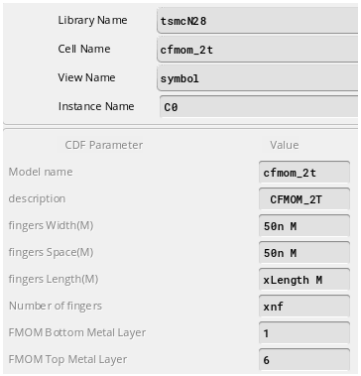

| Test | Output | Min | Max | Mean | Median | Std Dev | Spec | Pass/Fail |
|---|---|---|---|---|---|---|---|---|
| AMSdesign2025:NMOS_mirror:1 | Id_MNA | 9.998u | 10.02u | 10u | 10u | 5.744n | | |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNA | 453.3m | 494.4m | 475.8m | 475.5m | 7.876m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNA | 465.6m | 504.8m | 487.4m | 487.4m | 7.789m | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNA | 92.89m | 96.15m | 94.3m | 94.26m | 655.1u | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNA | 371.4m | 411.2m | 393.1m | 393m | 7.807m | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNA | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB | 9.522u | 10.43u | 9.98u | 9.985u | 187.3n | range 9u 11u | pass |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNB | 453m | 496.3m | 475.8m | 475.6m | 7.837m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNB | 400m | 400m | 400m | 400m | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNB | 91.94m | 96.65m | 94.31m | 94.32m | 865.3u | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNB | 303.3m | 308.1m | 305.7m | 305.7m | 865.3u | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNB | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNC | 9.514u | 10.65u | 9.982u | 9.971u | 194.4n | range 9u 11u | pass |
| AMSdesign2025:NMOS_mirror:1 | Vth_MNC | 453.6m | 495.5m | 475.8m | 475.5m | 7.807m | | |
| AMSdesign2025:NMOS_mirror:1 | Vds_MNC | 400m | 400m | 400m | 400m | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Vdsat_MNC | 91.82m | 96.5m | 94.32m | 94.32m | 922.6u | | |
| AMSdesign2025:NMOS_mirror:1 | Vsat_marg_MNC | 303.5m | 308.2m | 305.7m | 305.7m | 922.6u | > 200m | pass |
| AMSdesign2025:NMOS_mirror:1 | OP_region_MNC | 2 | 2 | 2 | 2 | 0 | | |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNB_error | -433.9n | 482.6n | 24.26n | 18.13n | 187n | range -300n 300n | fail |
| AMSdesign2025:NMOS_mirror:1 | Id_MNA_MNC_error | -652.8n | 485n | 21.26n | 30.2n | 194.4n | range -300n 300n | fail |
| AMSdesign2025:NMOS_mirror:1 | Id_MNB_MNC_error | -568.2n | 623.6n | -2.992n | -7.188n | 188.1n | range -300n 300n | fail |

# 7. Capacitor's Mismatch

## 7.1. schematic

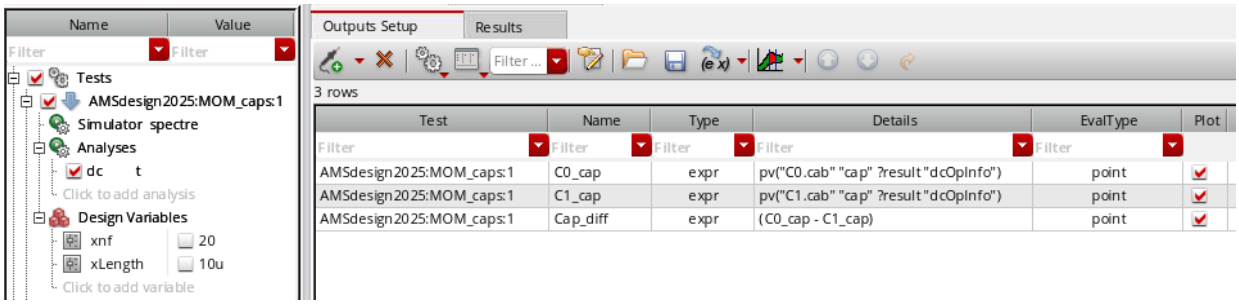
Create a new schematic and instance 2 Metal-oxide-Metal (MOM) capacitors from TSMC28 PDK technology and connect them to a voltage source with 0.9V DC voltage value. Give variable names to the number of fingers (eg. xnf) and Length of each finger (eg. xLength). See example below.



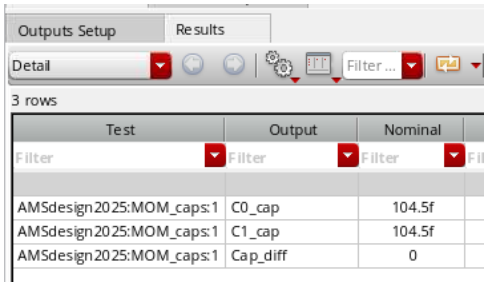




## 7.2. Create a Maestro ADE and run process corner simulations

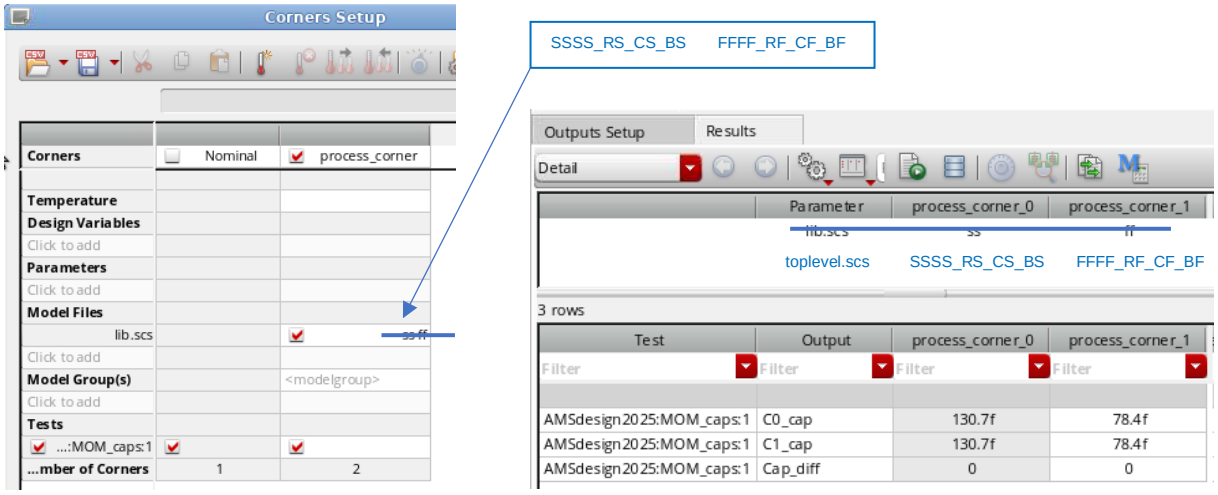
Create a new Maestro ADE. Select DC analyses. Run a typical process (section "TTTT_RT_CT_BT") and temperature (27ºC) and save the capacitors values from "dcOpInfo" simulation to ADE (if necessary, revisit point 3.6 above on how to add expressions to ADE). See example below:




Refresh results tab to see capacitors values. See example below:



Add “SSSS_RS_CS_BS” and “FFFF_RF_CF_BF” process corner variations and run the simulations.



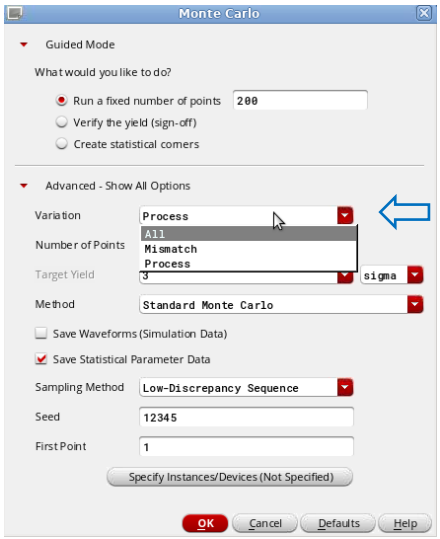

Compare the capacitors values for the different process corners.

- A total balanced variation of ±25% is observed.

As expected, there is no difference between their values because mismatch variation has not been added.

## 7.3. Run Monte-Carlo variation corners

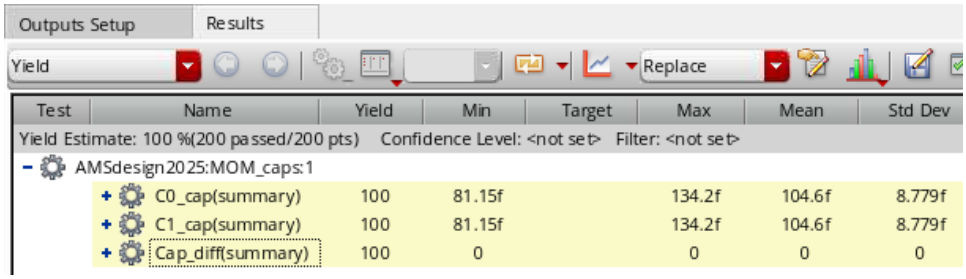
Select Monte-Carlo simulation. On model’s library configuration dialog box select “globalmc_localmc” section with 200 simulation points and run 3 simulations each one with a different type of variation (“Process”, ”Mismatch” and “All”).



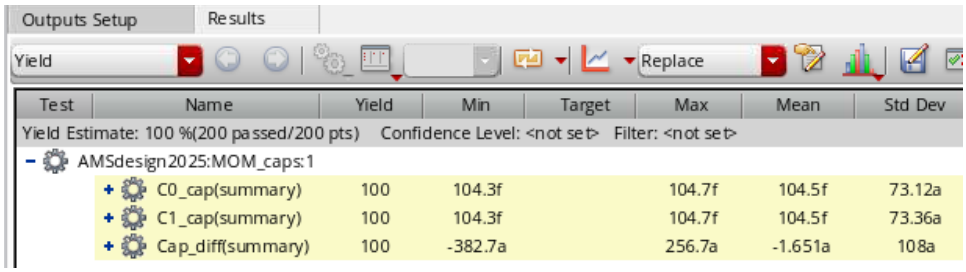

Select just Nominal corner:

See examples below of simulation results for the 3 different types of Monte-Carlo variations.

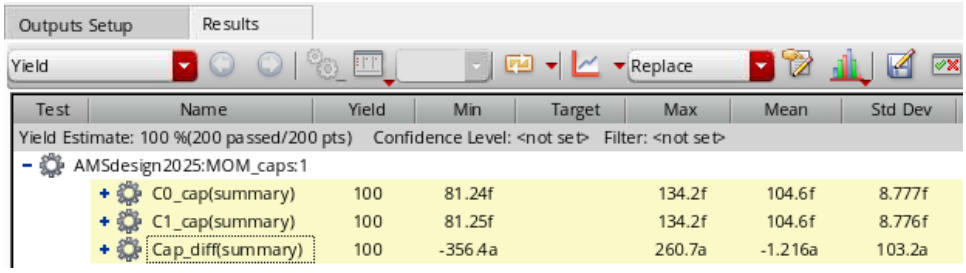
- “globalmc_localmc” section with global “Process” variation:




- “globalmc_localmc” section with local “Mismatch” variation:




- “globalmc_localmc” section with “All” (global Process + local Mismatch) variation:




Compare the results and conclude the impact of global Process and local Mismatch variations on capacitors' values.

For total corner variations the foundry uses the 3σ results. See calculations below for above simulation results.

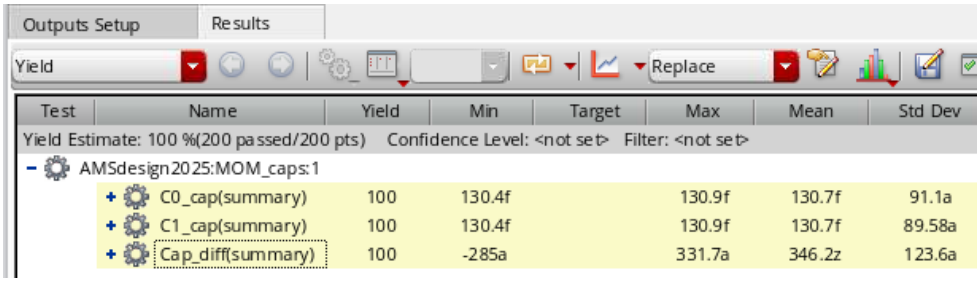
$$[\mu - 3\sigma\,;\ \mu + 3\sigma] = [104.6 - (3 \times 8.777)\,;\ 104.6 + (3 \times 8.777)]\ \text{fF} = [78.27\,;\ 130.93]\ \text{fF}$$

Let’s compare them with the total corner variations results obtained earlier:

$$[\text{ff};\ \text{tt};\ \text{ss}] = [78.4\,;\ 104.5\,;\ 130.7]\ \text{fF}$$

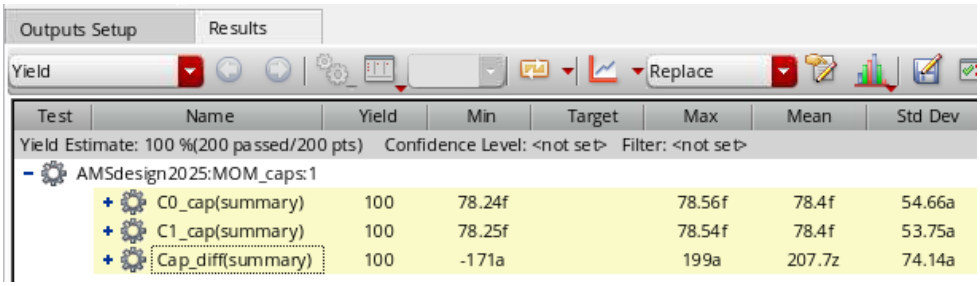
Change the model's sections to "SSSS_RS_CS_BS" and "FFFF_RF_CF_BF" and compare with the results above with "globalmc_localmc". See below example of simulation results.

- "SSSS_RS_CS_BS" section with "Mismatch" variation (SS Process + local Mismatch):




Note the results are centered on "SSSS_RS_CS_BS" process corner result (130.7fF) obtained on point 7.2.

- "FFFF_RF_CF_BF" section with "Mismatch" variation (FF Process + local Mismatch):

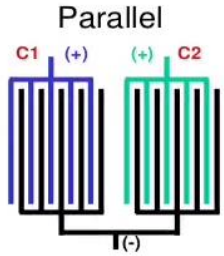



Note the results are centered on "FFFF_RF_CF_BF" process corner result (130.7fF) obtained on point 7.2.

## 7.4. Calculation of capacitor's matching parameter (Ac)

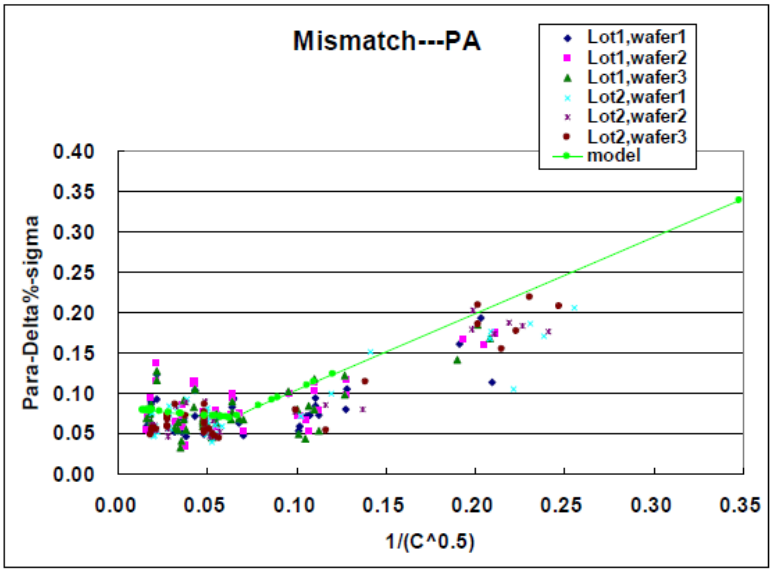
The capacitors mismatch has been modeled on the PDK spectre files with an Ac parameter according to the following formula.

$$\sigma\left(\frac{\Delta c}{C}\right) = \frac{Ac}{\sqrt{C}} \qquad [\%]$$




The Ac parameter was obtained on the foundry from silicon measurements of the difference between 2 parallel MOM devices capacitance values.

On the graphic below, present on TSMC devices mismatch information document, it is possible to see the 1 sigma statistical calculation percentage of the variation between 2 parallel capacitors values.




The Ac parameter will correspond to the slope of the linear regression (green line) calculated from the silicon results for different wafers.

Choosing two different capacitors sizes, for example 25fF ($\frac{1}{\sqrt{25}} = 0.2\ fF^{-0.5}$) and 100fF ($\frac{1}{\sqrt{100}} = 0.1\ fF^{-0.5}$) is possible to calculate the Ac.

$$Ac = \frac{0.2 - 0.1}{0.2 - 0.1} = 1 \qquad [\%.fF^{-0.5}]$$

The “Ac“ parameter can be used on the modeling of the DAC capacitors mismatch variation (for example in an ADC Matlab behavior modelling script). The results can then be used on the definition of the DAC capacitors calibration corrections factors for a good ADC DNL/INL linearity.

The standard variation of the difference between the 2 random capacitors values is given by:

$$\sigma(\Delta c) = \sigma(c_1 - c_2) = \sqrt{\sigma^2(c_1) + \sigma^2(c_2) + cov(c_1, c_2)}$$

Assuming the standard variations values of $c_1$ and $c_2$ are independent, the covariance is canceled.

$$\sigma(\Delta c) = \sqrt{\sigma^2(c_1) + \sigma^2(c_2)} = \sqrt{2 \cdot \sigma_n^2} = \sqrt{2} \cdot \sigma_n$$

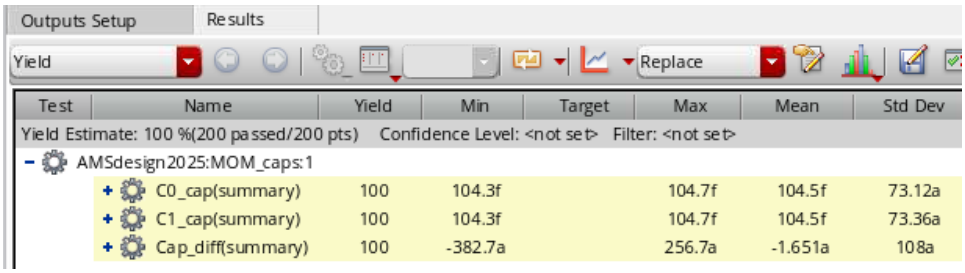
Dividing by normalized capacitor value $C_n$ is possible to obtain the variation of a capacitor value from the Ac and respective capacitor mean value:

$$\sigma\left(\frac{\Delta c}{C}\right) = \sqrt{2} \cdot \frac{\sigma_n}{C_n} \quad \Leftrightarrow \quad \frac{\sigma_n}{C_n} = \sigma\left(\frac{\Delta c}{C}\right) \cdot \frac{1}{\sqrt{2}} \quad \Leftrightarrow \quad \frac{\sigma_n}{C_n} = \frac{Ac}{\sqrt{C_n}} \cdot \frac{1}{\sqrt{2}} \quad \Leftrightarrow \quad \sigma_n = \frac{Ac}{\sqrt{C_n}} \cdot \frac{1}{\sqrt{2}} \cdot C_n$$

With the above formula it is possible to obtain an estimation of the standard deviation for the capacitor value:

$$\sigma_{(104.5fF)} = \frac{0.01}{\sqrt{104.5}} \cdot \frac{1}{\sqrt{2}} \cdot 104.5 = 0.0723\ fF$$

As can be seen from the table below, the resulting value is similar with the standard deviation obtained from Monte-Carlo local “Mismatch” simulation (obtained on point 7.3 simulations above). See respective simulation results below:




Monte-Carlo simulation results with “globalmc_localmc” section and local “Mismatch” variation.

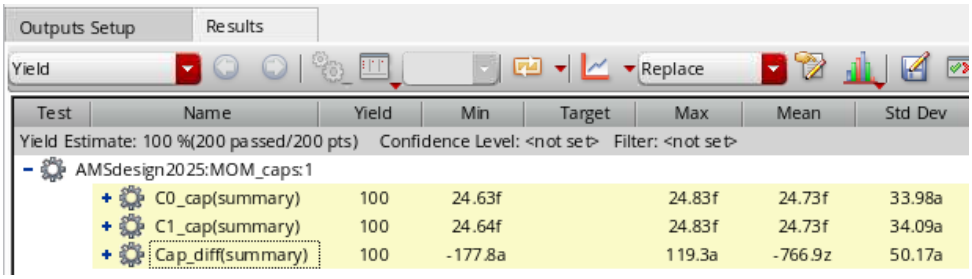
(xnf=20 ; xLength=10u)

In case the access to foundry documentation is not possible, the Ac parameter can be obtained from Monte-Carlo local mismatch simulation results.
Let’s consider the Monte-Carlo local “Mismatch” simulation results above.

$$Ac = \sigma\left(\frac{\Delta c}{C}\right) \cdot \sqrt{C} = \frac{0.108}{104.5} \cdot \sqrt{104.5} = 1.06 \quad [\%.fF^{-0.5}]$$

The Ac results match with the value taken from TSMC documentation plot.

Re-running the Monte-Carlo with smaller capacitors sizes. From example below with xnf=10 and xLength=5u, it is possible to see the Ac parameter has not changed significantly, which indicates we can use the Ac parameter independent from the unit capacitor size/value to estimate the mismatch between 2 distinct capacitors.




Monte-Carlo simulation results with “TTTT_RT_CT_BT” section and local “Mismatch” variation.

(xnf=10 ; xLength=5u)

$$Ac = \sigma\left(\frac{\Delta c}{C}\right) \cdot \sqrt{C} = \frac{0.05017}{24.73} \cdot \sqrt{24.73} = 1.01 \quad [\%.fF^{-0.5}]$$

The calculation of the capacitor value standard deviation from the Ac value, for the smaller sized capacitor, can also be confirmed to match with simulation results:

$$\sigma_{(24.73fF)} = \frac{0.01}{\sqrt{24.73}} \cdot \frac{1}{\sqrt{2}} \cdot 24.73 = 0.0352\ fF$$

A stable Ac is inline with the expectation that a smaller sized capacitor will have a higher mismatch value between 2 parallell structures. From the formula it can be seen the sigma (σ) has an inverse relation with the $\sqrt{C}$.

From the examples above, it can be seen, the mismatch is 2 times bigger for the smaller sized capacitors wen compared with the mismatch between the two bigger capacitors.

$$\frac{c(3\sigma)}{C}_{Bigger\ Size} = \frac{3 \times 0.07312fF}{104.5fF} = 0.21\ [\%] \quad ; \quad \frac{c(3\sigma)}{C}_{Smaller\ Size} = \frac{3 \times 0.03398fF}{24.73fF} = 0.41\ [\%]$$

## 7.5. How to save data in Monte-Carlo simulation

By default, the Monte-Carlo simulation does not save the simulation data to reduce disk space usage. Without saving them it is not possible to plot signals or run new post simulation calculations.
To be able to save the data on Monte-Carlo simulations, open respective configuration dialog box and select “Save Waveforms (Simulation Data)”.