MODULE 4 – PIPELINE ADCS

JULY 2025

RENESAS ELECTRONICS CORPORATION

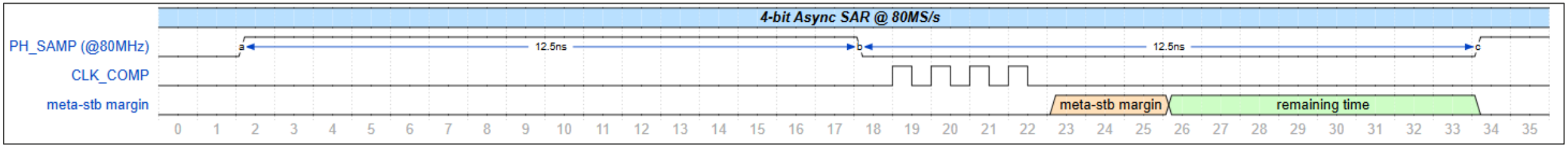
AGENDA

- Start from the 4-bit SAR ADC designed on the previous module workshop.
- Move from there to understand the SAR architecture limitations.
- Get into Pipeline ADC architectures and understand how it overcomes the SAR limitations.
- Practical examples to understand key design aspects from the pipeline architecture:
  - Residue Amplification and Inter-Stage Gain
  - Digital Correction
  - Effects of the STG1 Capacitors Mismatch on the ADC DNL/INL

A PRACTICAL PERSPECTIVE ON PIPELINE ADCS

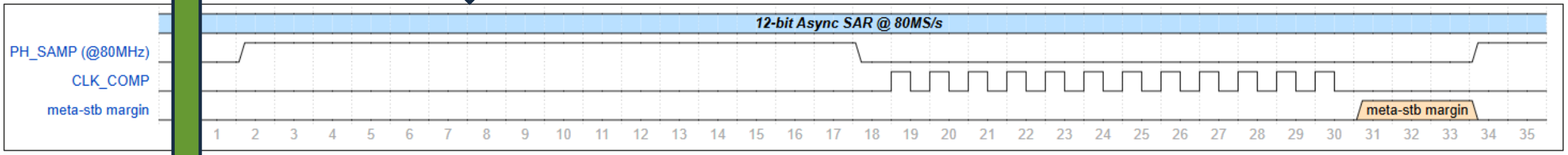
SAR ADC TIMING (EXAMPLE BASED ON THE WORKSHOP)

4-bit SAR-ADC @ 80MS/s (Workshop Exercise)



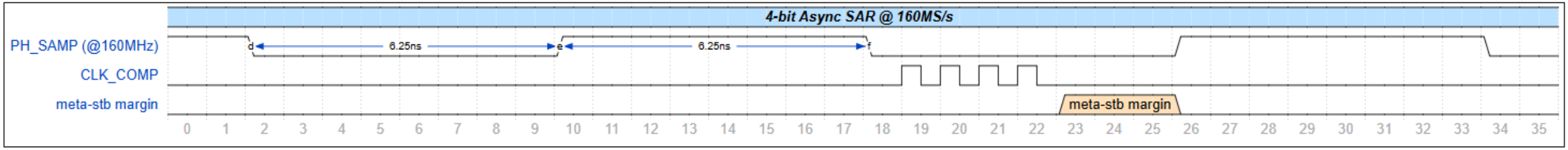
Insert additional bits

12-bit SAR-ADC @ 80MS/s

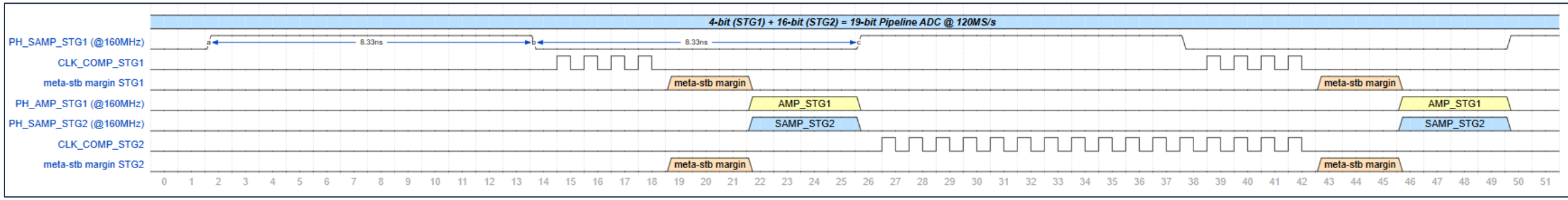


Increase the sampling frequency

4-bit SAR-ADC @ 160MS/s

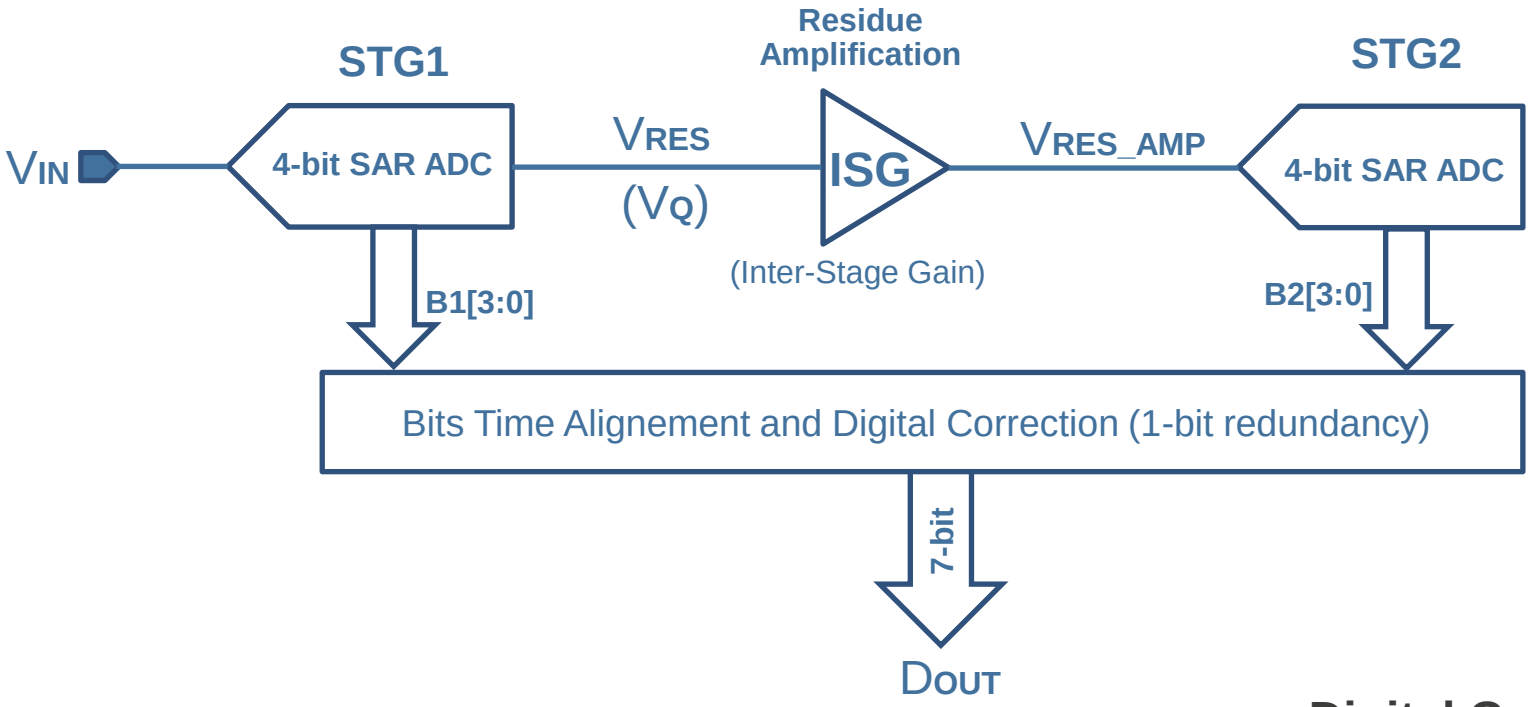


PIPELINE ADC TIMING (EXAMPLE BASED ON THE WORKSHOP)

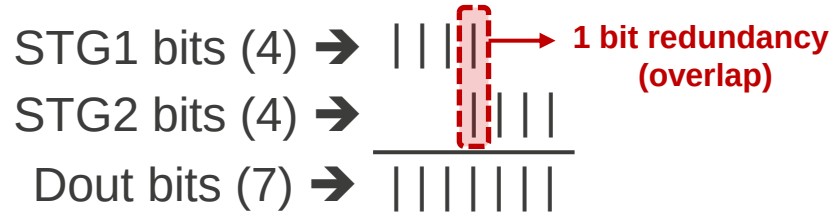


- STG1 quantizes 4-bit and amplifies the residue voltage (Vres) ➔ STG1 reaches 120MS/s operating frequency.
- STG2 gets and extended time slot for quantization.
  (due to reduced duty cycle on STG2 sampling phase, which matches STG1 amplification phase).
- STG2 manages to quantize 16-bit with the extend time slot it has available (optimistically considering the average easy decisions time would be maintained... while in practice it would not happen, because STG2 Vres is much smaller, therefore the comparator's decisions will be slower).
- Being more realistic... it is reasonable to think STG2 may be able to quantize ~9 bit @120MS/s.
- Summing STG1 and STG2 bits (with 1-bit redundancy) results in a 12-bit ADC @ 120MS/s

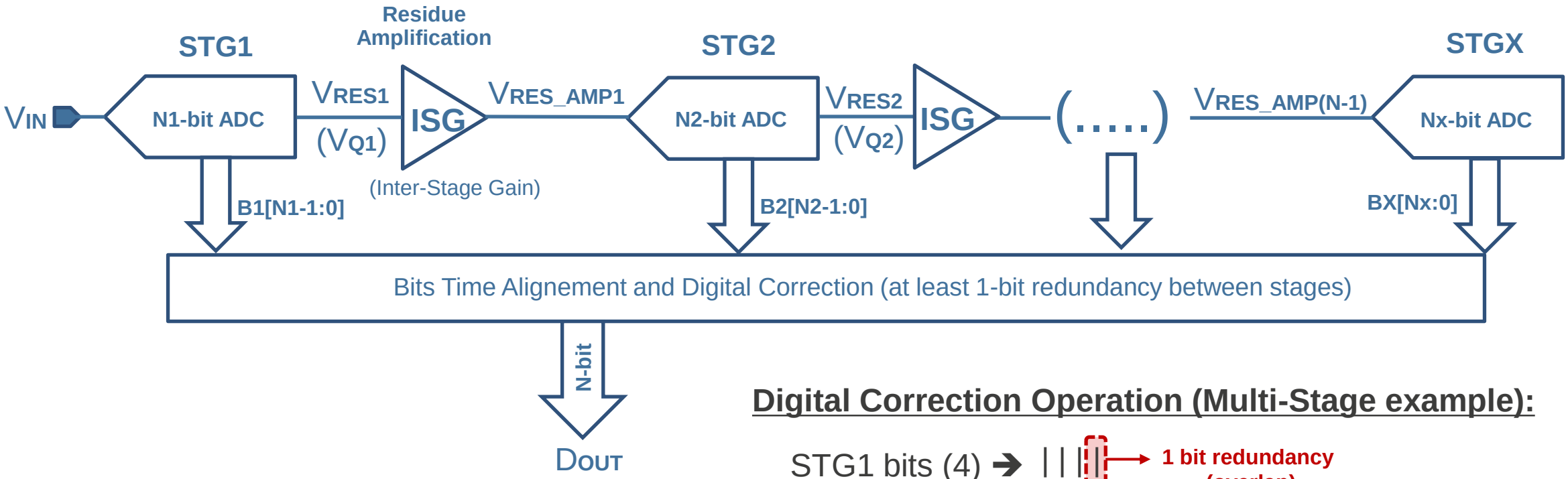
PIPELINE ADC STRUCTURE (2 STAGES, EXAMPLE)



Digital Correction Operation:

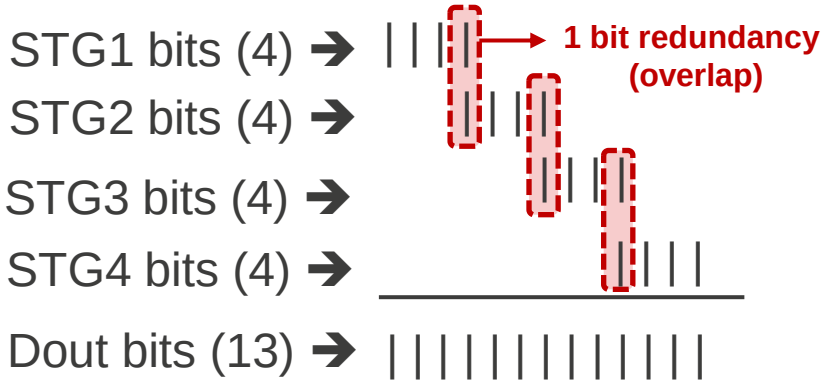


PIPELINE ADC STRUCTURE (N STAGES, GENERIC)

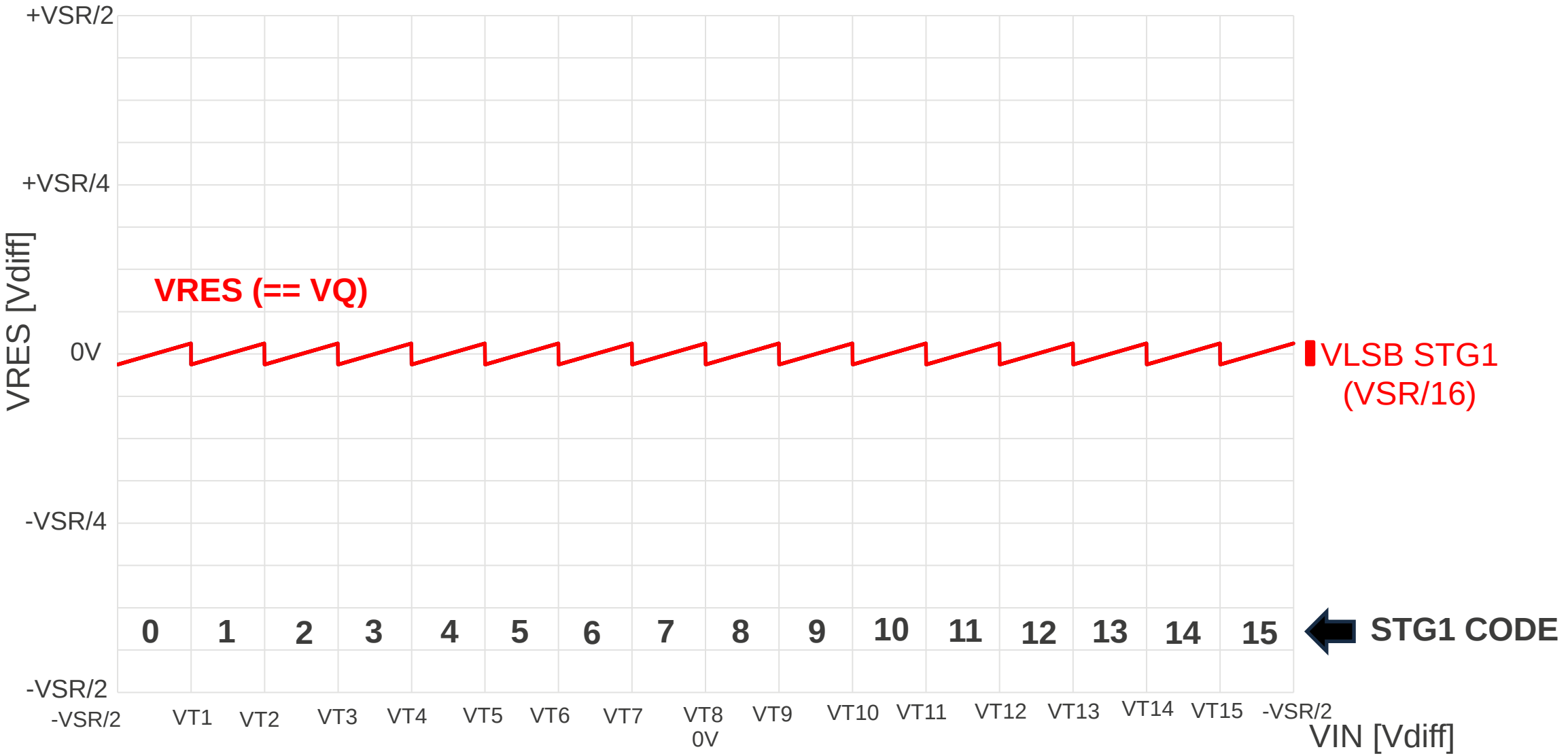


The stages quantization does not need necessarily to be SAR based.
It can be Flash based, or TDC based, or any other type.

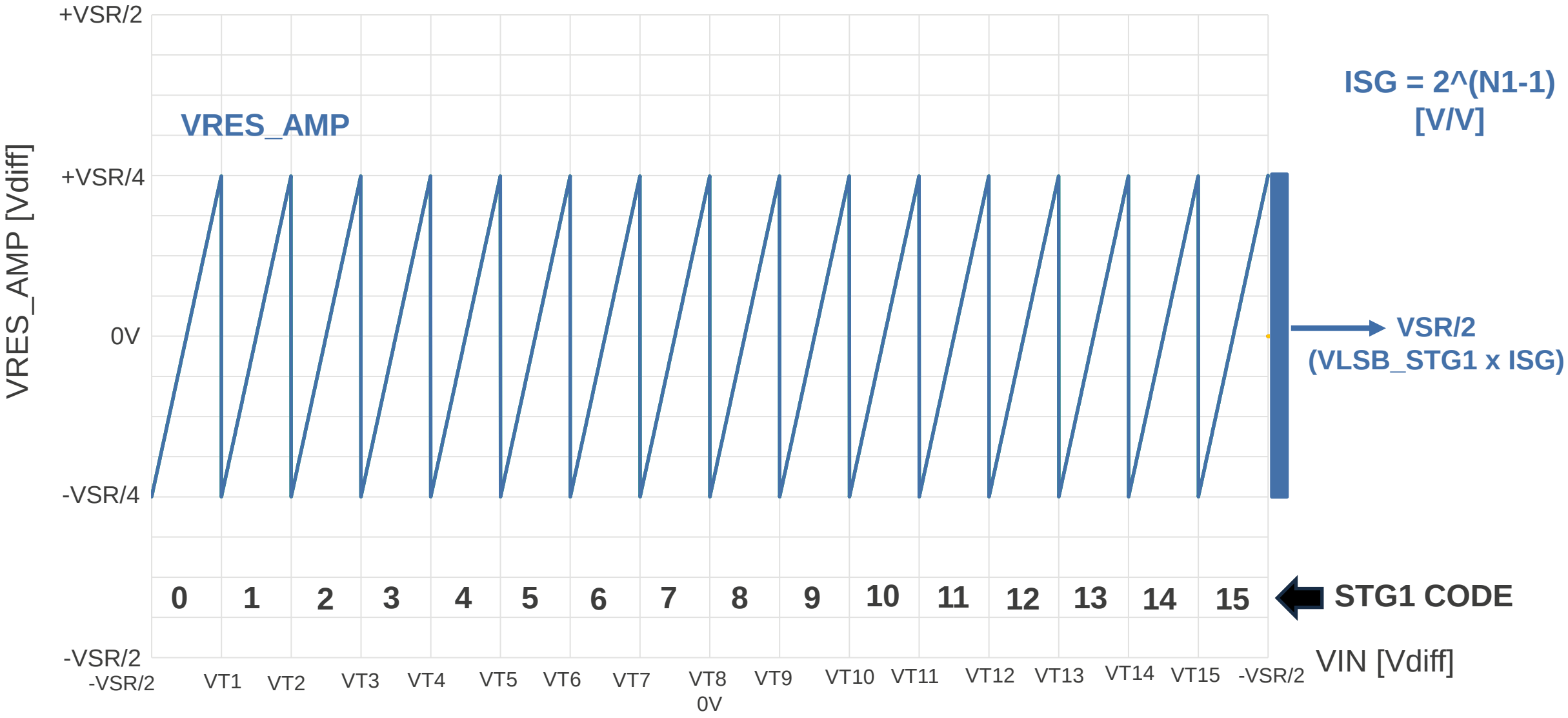
Digital Correction Operation (Multi-Stage example):



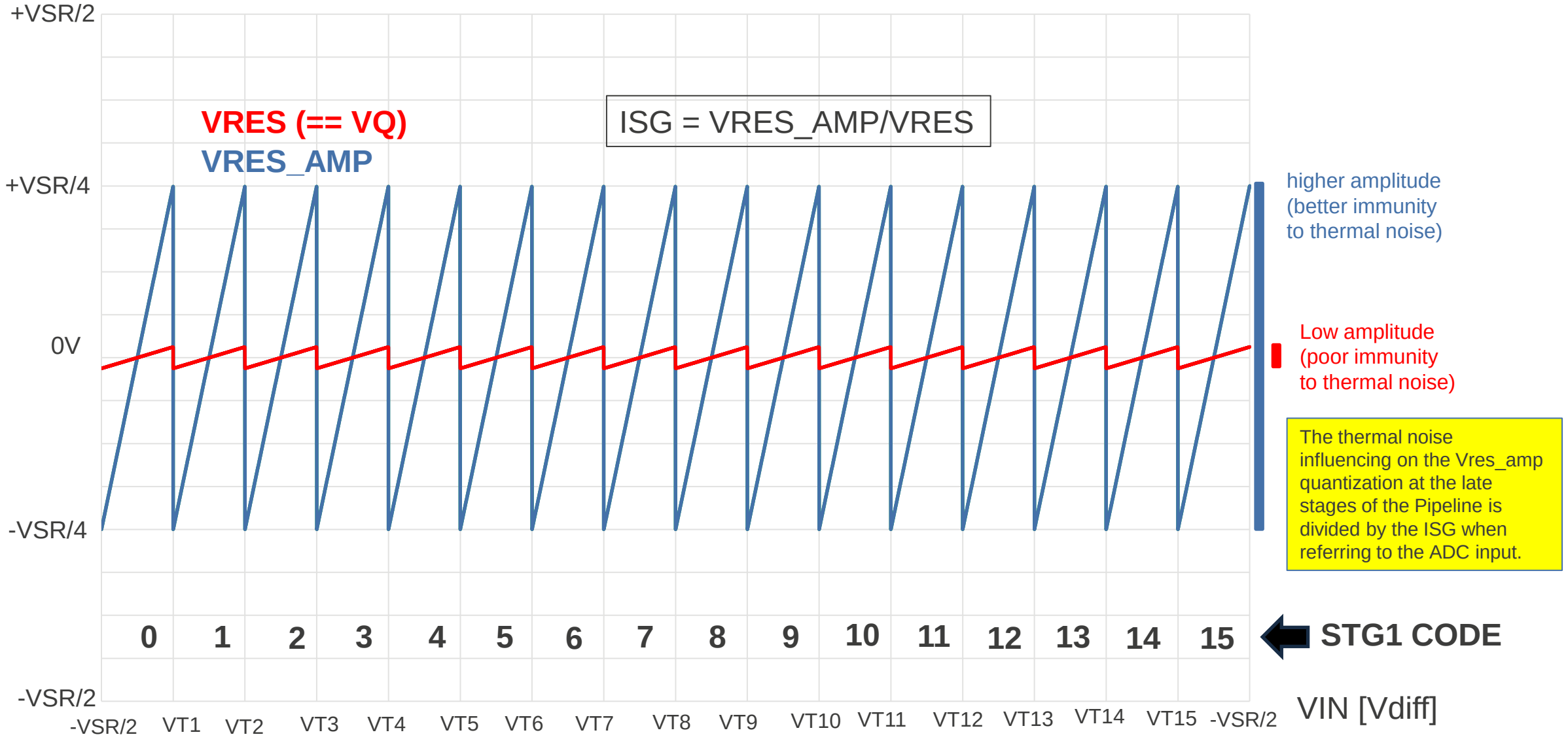
4-BIT STG1 TRANSFER FUNCTION – VRES (VIN)



4-BIT STG1 AMPLIFIED TRANSFER FUNCTION - VRES_AMP(VIN)



COMPARING VRES AND VRES_AMP – THE NOISE ADVANTAGE



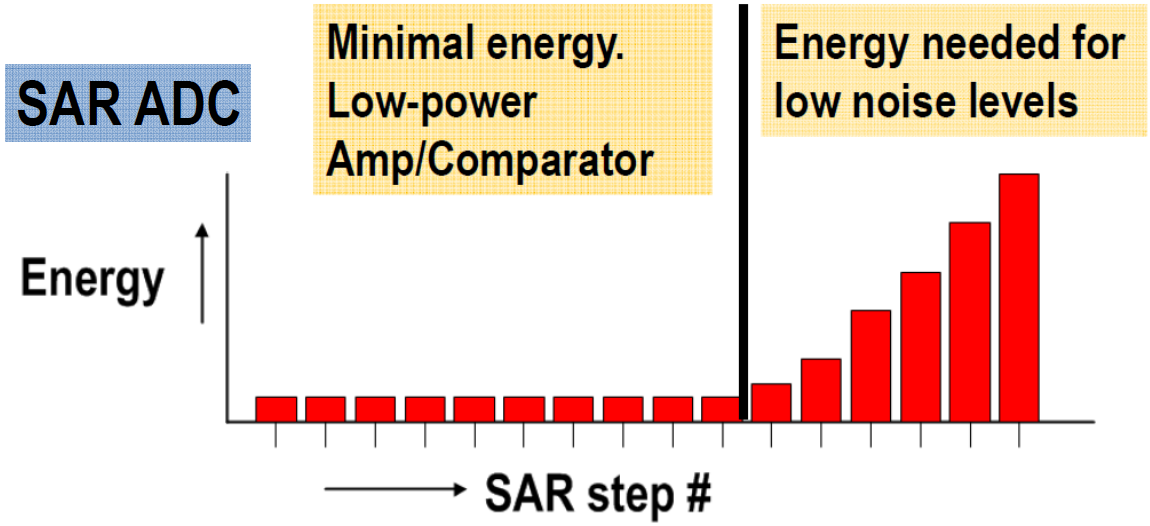
PIPELINE NOT ONLY FASTER BUT ALSO MORE POWER EFFICIENT

Pipelining → good power-efficiency for noise

SAR ADC → good power-efficiency for large signals

ISSCC2014 – BROADCOMM PAPER

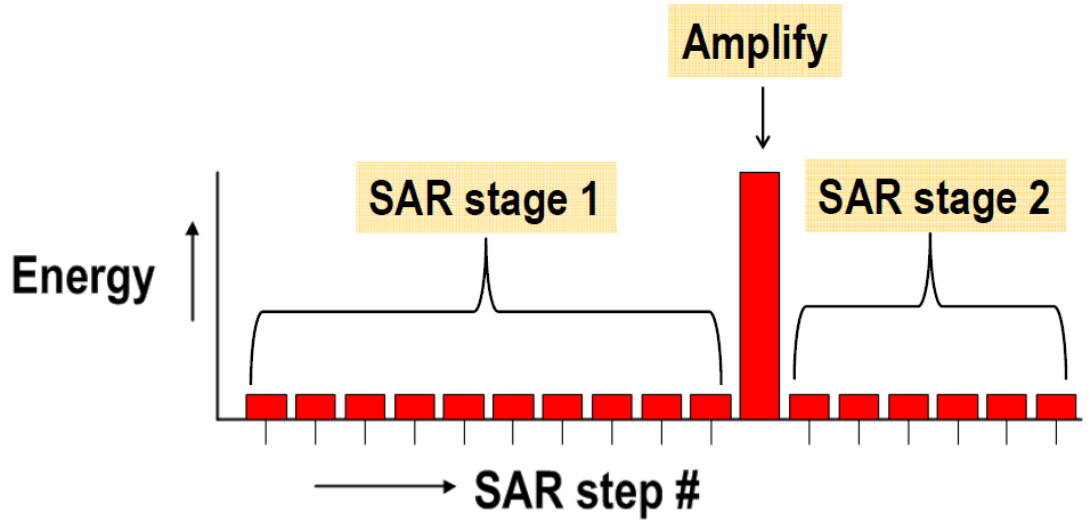
Required Energy to bring down Noise Level



Multiple high-energy (low-noise) events

SAR-assisted pipelined ADC can do better !

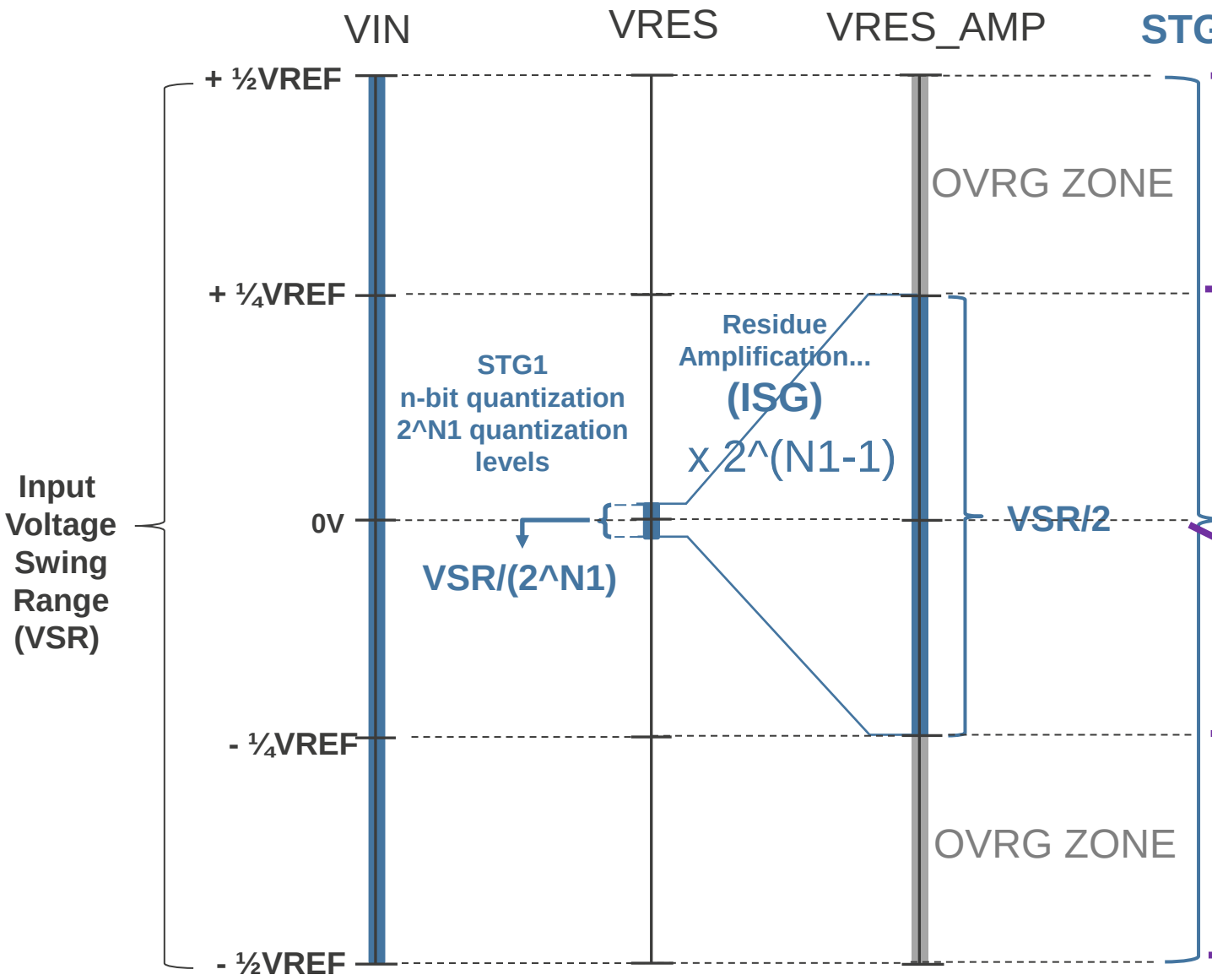
Required Energy of SAR-assisted Pipelined ADC



Low noise level is required only once

1 high-energy event: increased power efficiency wrt SAR

RESIDUE VOLTAGE AMPLIFICATION AND INTER-STAGE GAIN (ISG)



STG2 CODE = (2^N2) - 1

- The Over-Range Zones (OVRG) are necessary to deal with the STG1 comparator offset and/or incomplete settling on the DAC, which can cause quantization errors on STG1 code.

STG2 CODE = (3/4)*(2^N2)

The ISG value needs to be accurate, otherwise STG1 and STG2 quantization weights get misaligned and linearity errors happen in the Pipeline ADC.

VSR (STG2 Full Quantization Range)

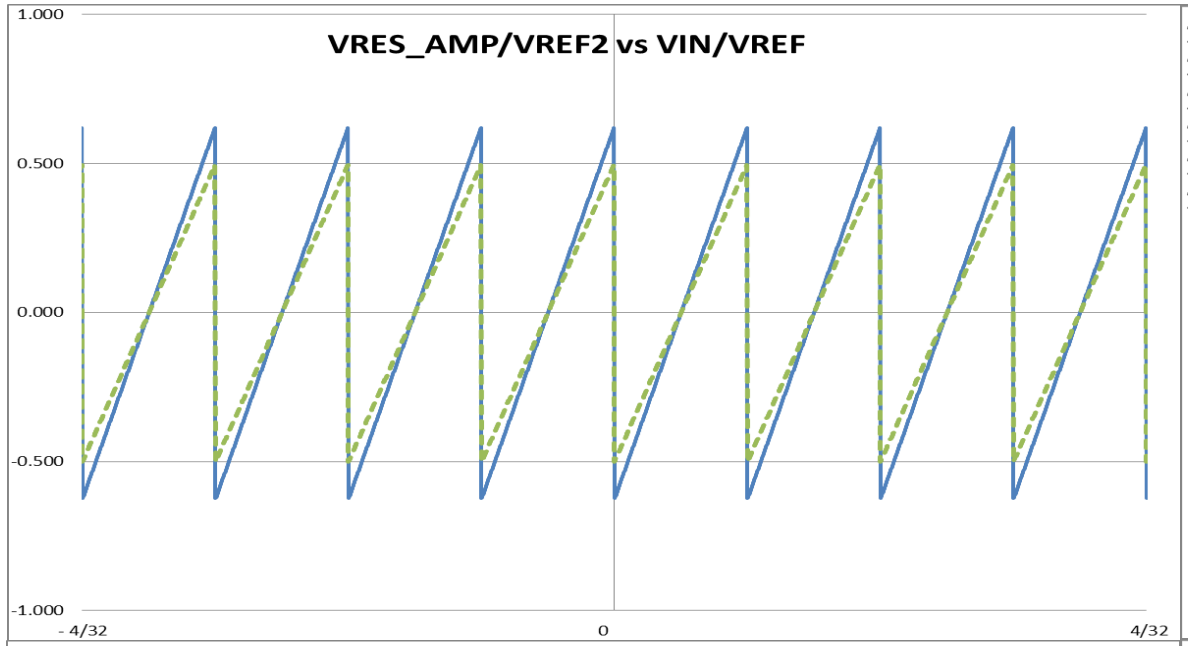
STG2 CODE = (1/2)*(2^N2)

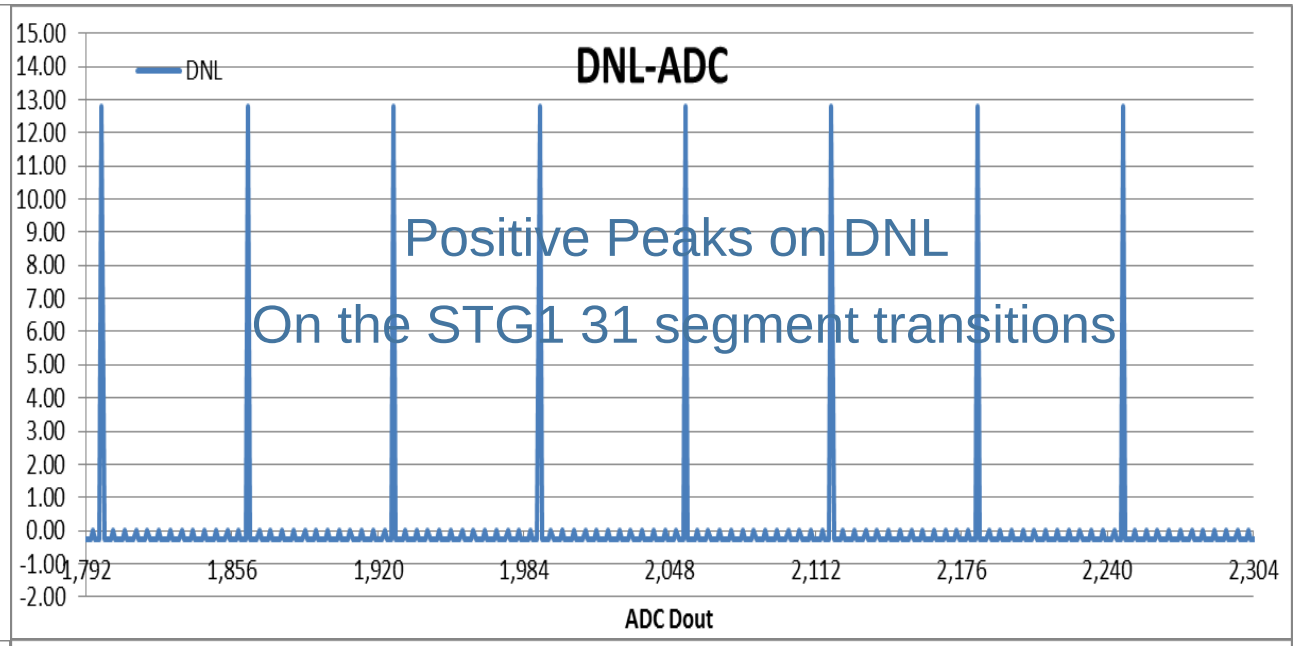
STG2 CODE = (1/4)*(2^N2)

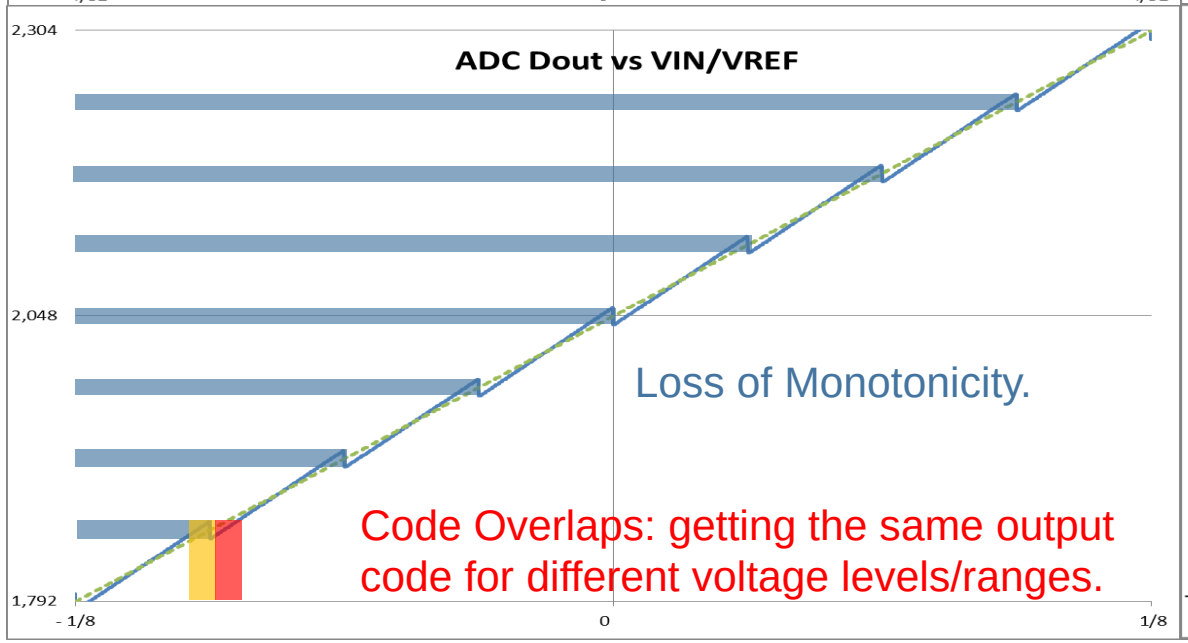
- Using the redundancy bit between the stages the digital correction circuitry can recover the quantization errors on STG1 code.

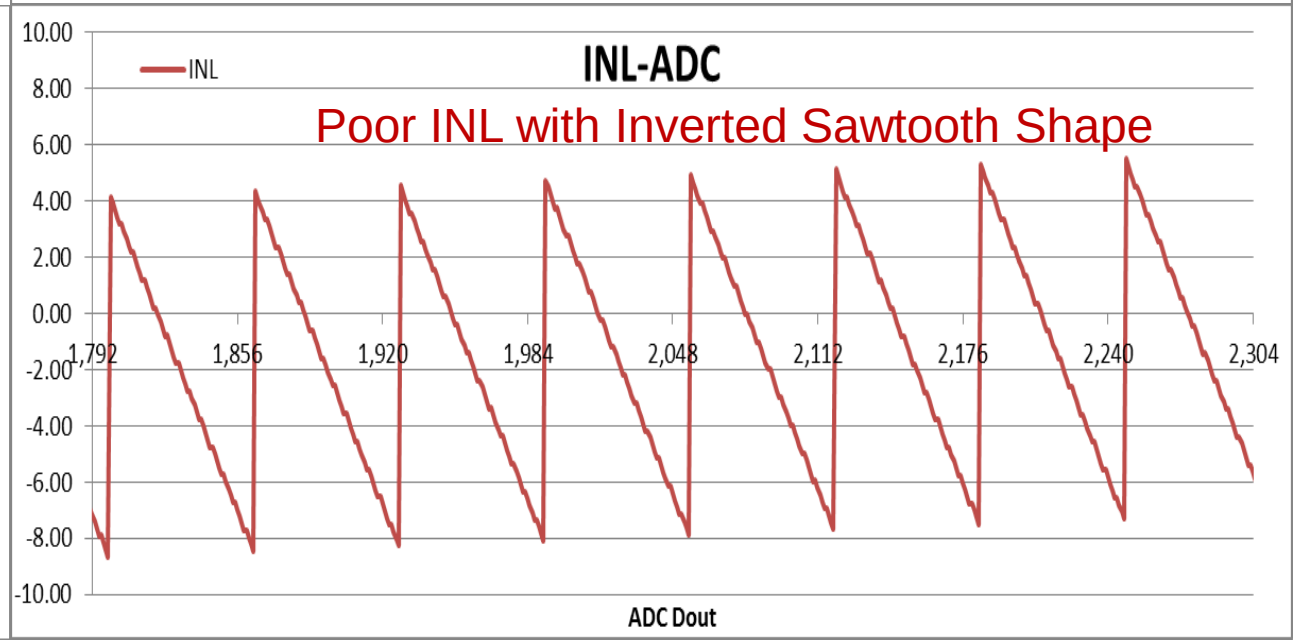
STG2 CODE = 0

EXCESS ISG ERROR AND ITS INFLUENCE ON THE ADC LINEARITY

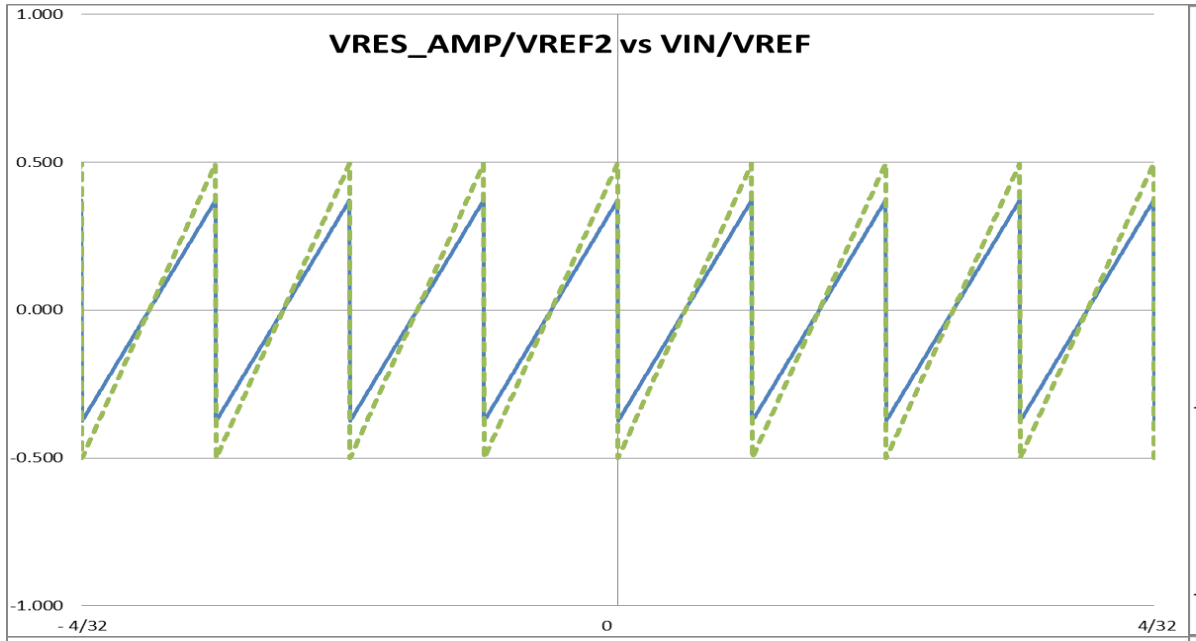


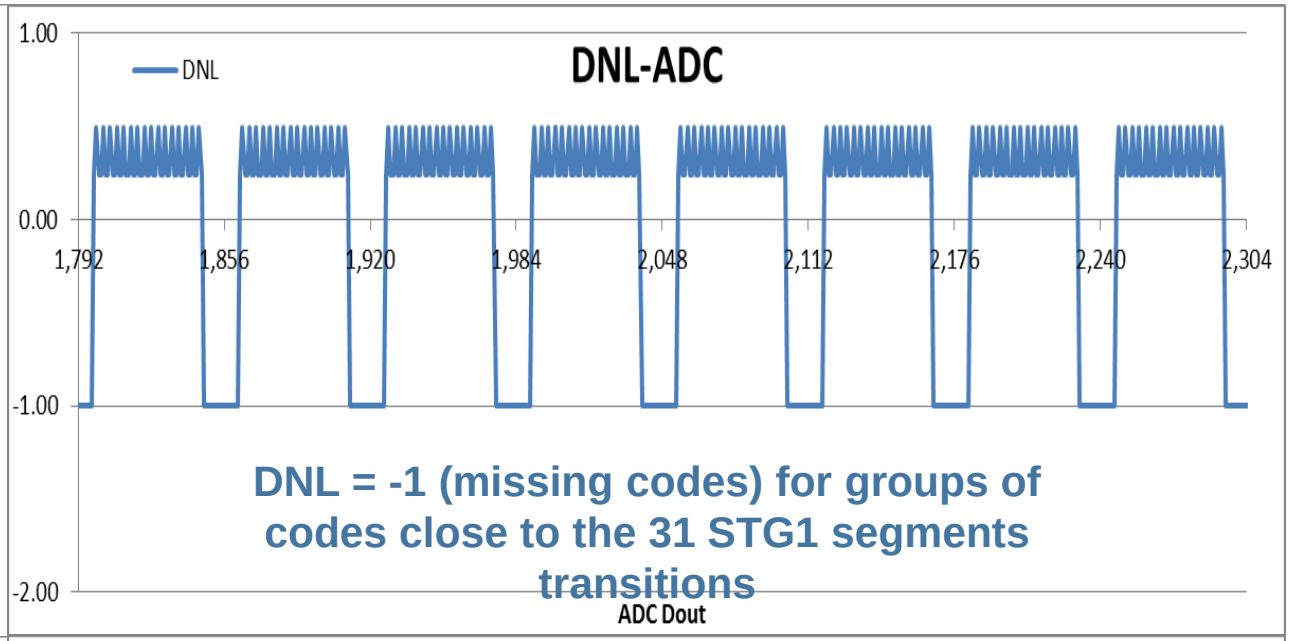




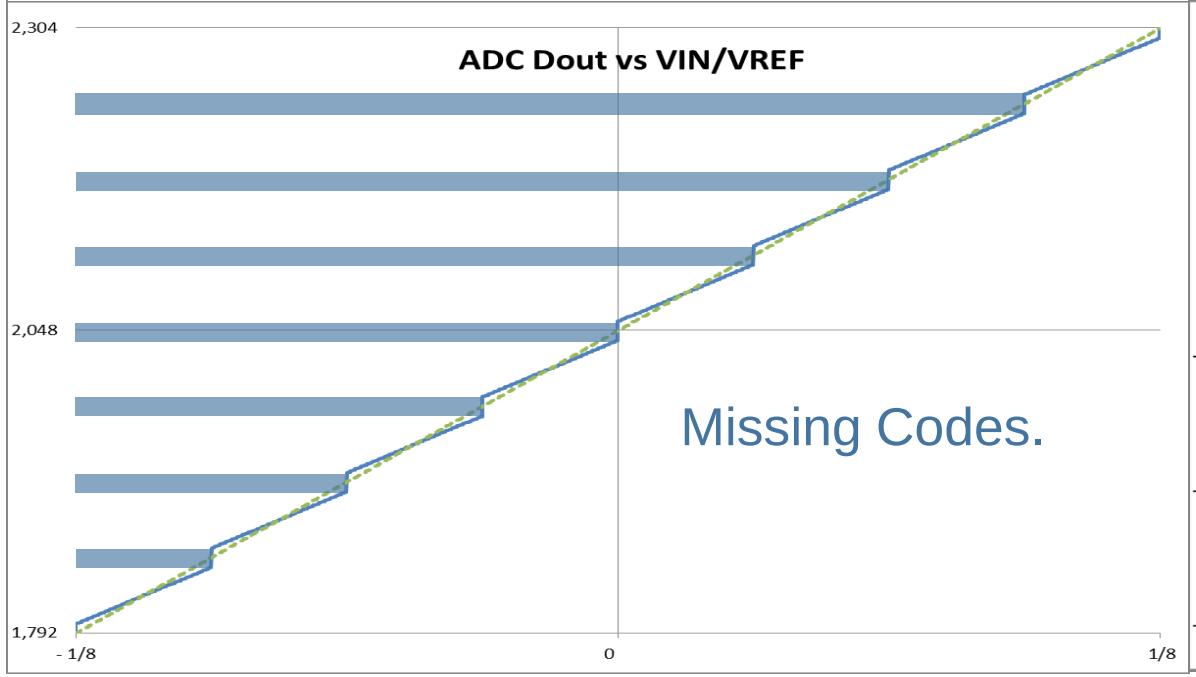


REDUCED ISG ERROR AND ITS INFLUENCE ON THE ADC LINEARITY

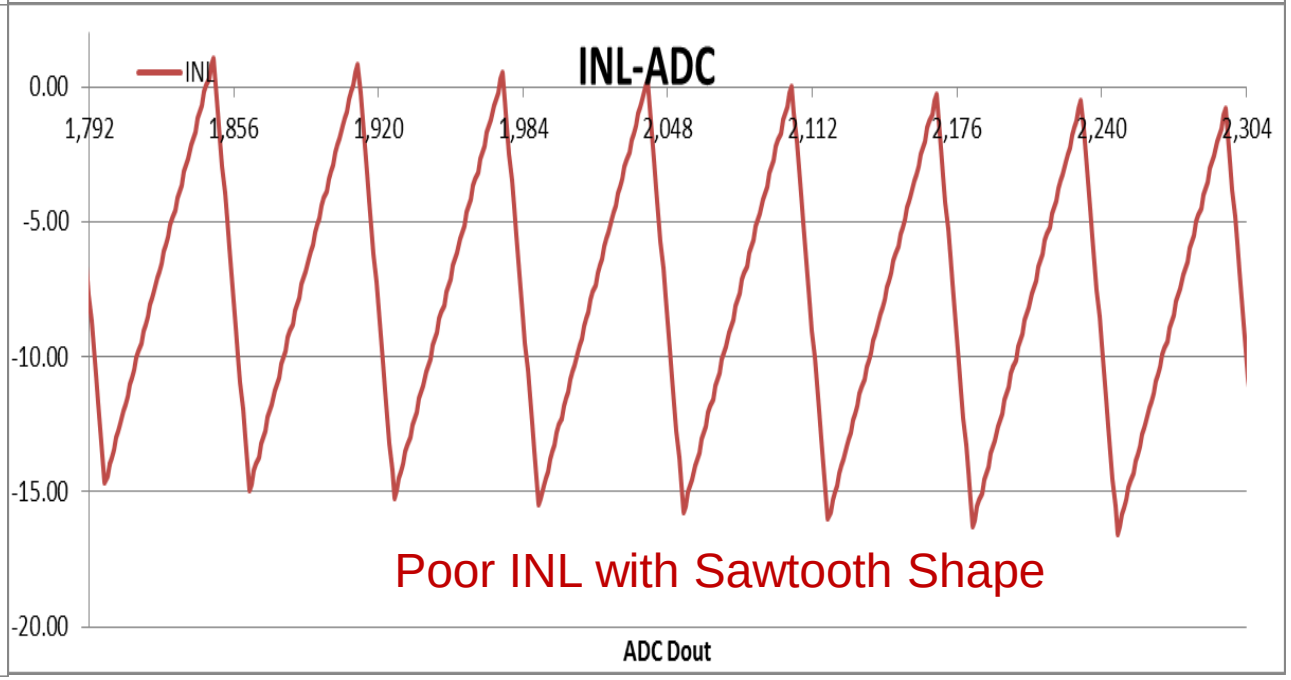




DNL = -1 (missing codes) for groups of codes close to the 31 STG1 segments transitions

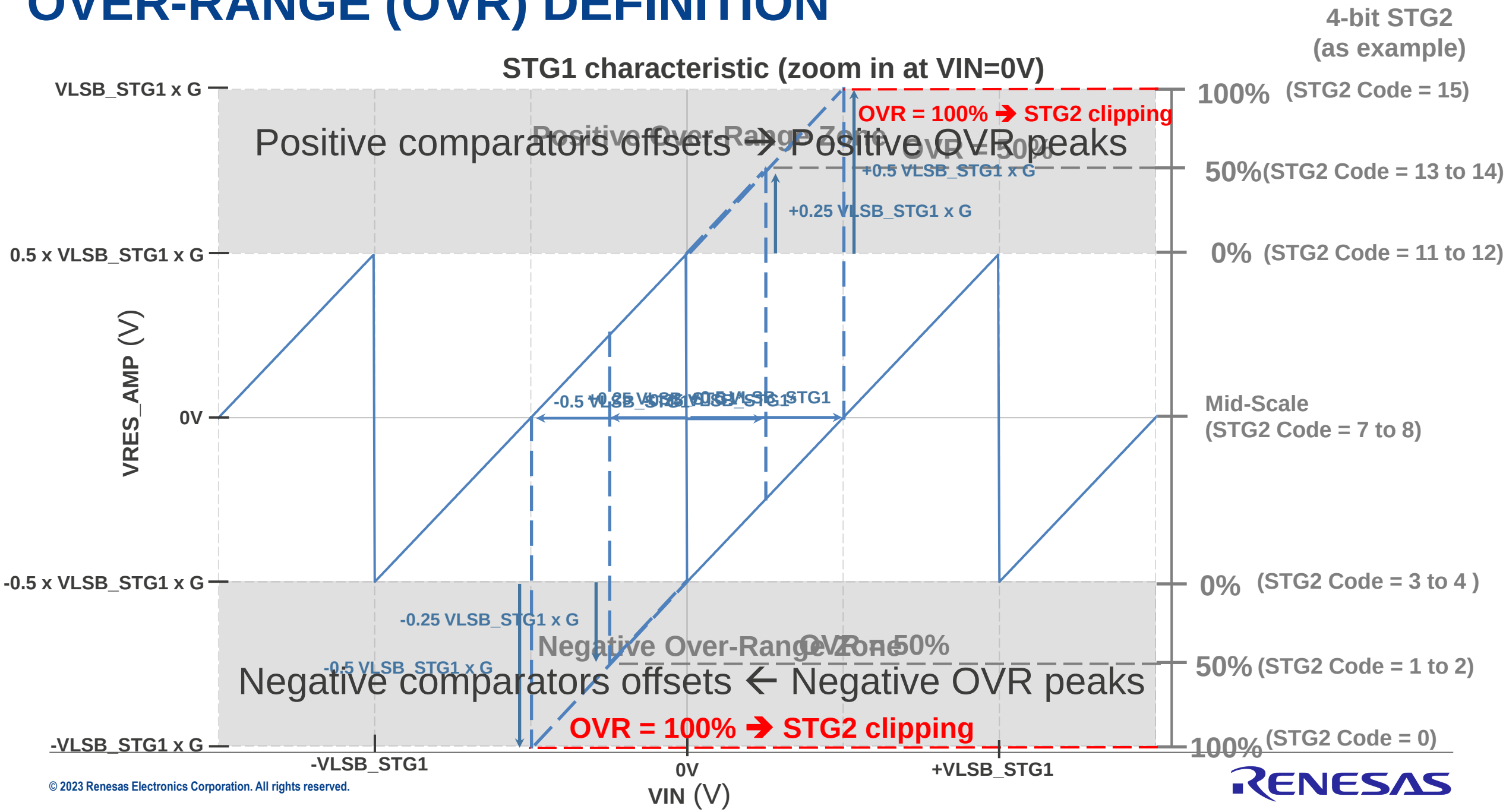


Missing Codes.



Poor INL with Sawtooth Shape

OVER-RANGE (OVR) DEFINITION



Positive comparators offsets → Positive OVR peaks

Negative comparators offsets ← Negative OVR peaks

THE DIGITAL CORRECTION OPERATION

- The ADC output code (Dout) is computed by the Digital Correction Circuit, combining the different stages bits.
- For a Two-Stage Pipeline ADC (mid-rise) the Digital correction equation is the following:

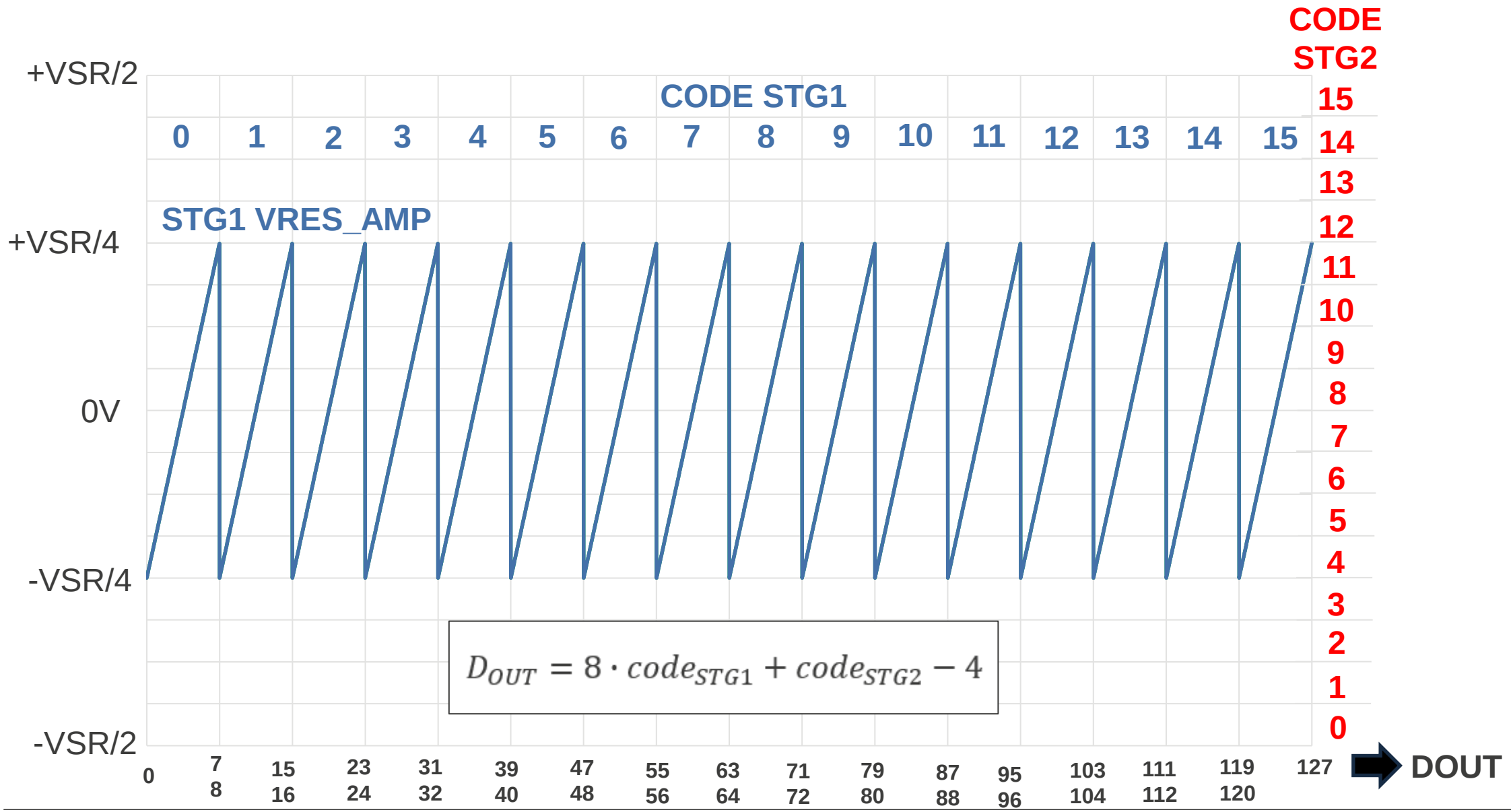
$$D_{OUT} = 2^{(N2-1)} \cdot code_{STG1} + code_{STG2} - 2^{(N2-2)}$$

- In the example of the workshop, we have N1=4-bit and N2=4-bit, so we get:

$$D_{OUT} = 8 \cdot code_{STG1} + code_{STG2} - 4$$

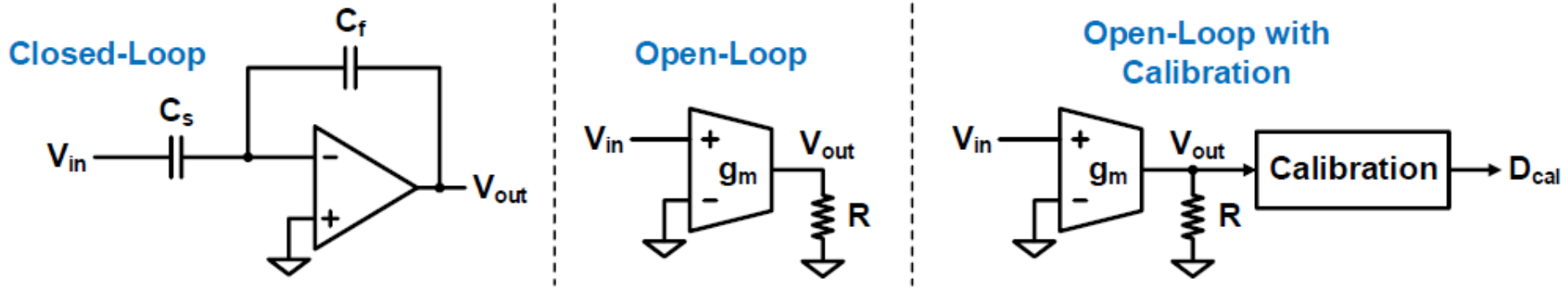
- Next slide we check an example on how the digital correction and the inter-stages redundancy bit works to correct STG1 quantization code errors.

4-BIT STG1 + 4-BIT STG2 EXAMPLE OF THE DIGITAL CORRECTION MAGICS



RESIDUE AMPLIFICATION APPROACHES

Residue Amplifier



	Closed-Loop	Open-Loop	Open-Loop + Calibration
Gain Accuracy	☺	☹	☺
Linearity	☺	☹	☺
Speed	☹	☺	☺
Efficiency	☹	☺	☺
Stability	☹	☺	☺
Scaling Friendly	☹	☺	☺

[B. Murmann, *JSSC*, 2003]

24.1: A 12b 3GS/s Pipelined ADC with Gated-LMS-Based Piecewise-Linear Nonlinearity Calibration

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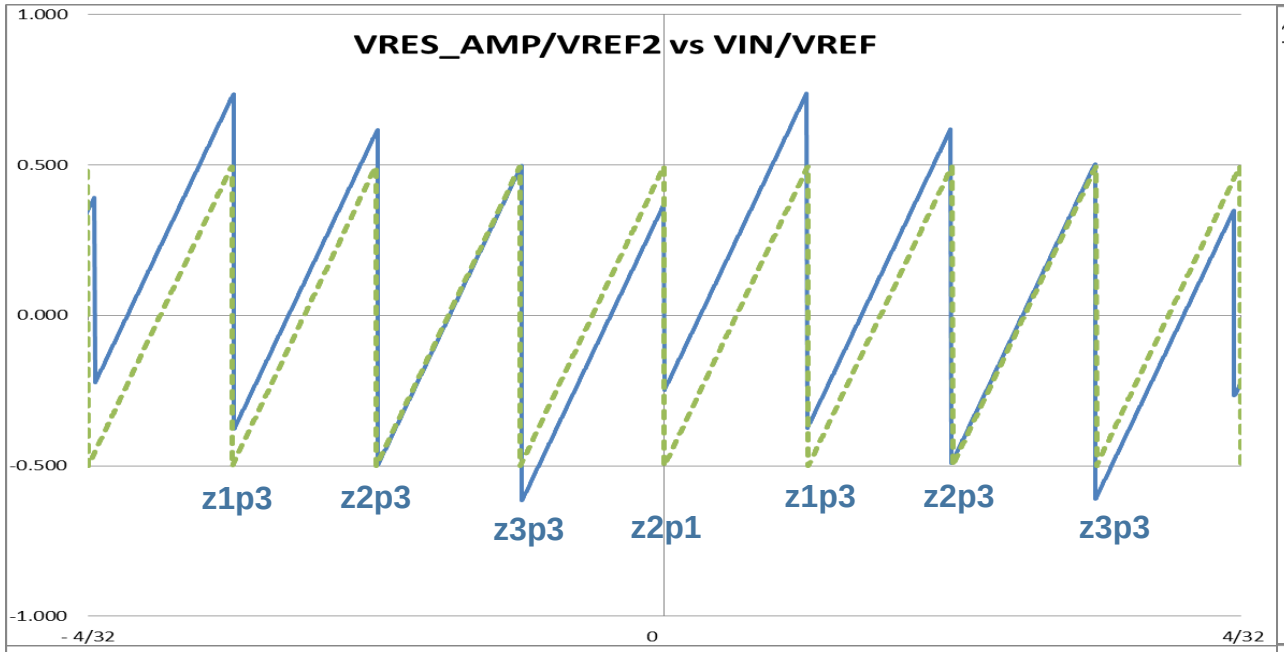
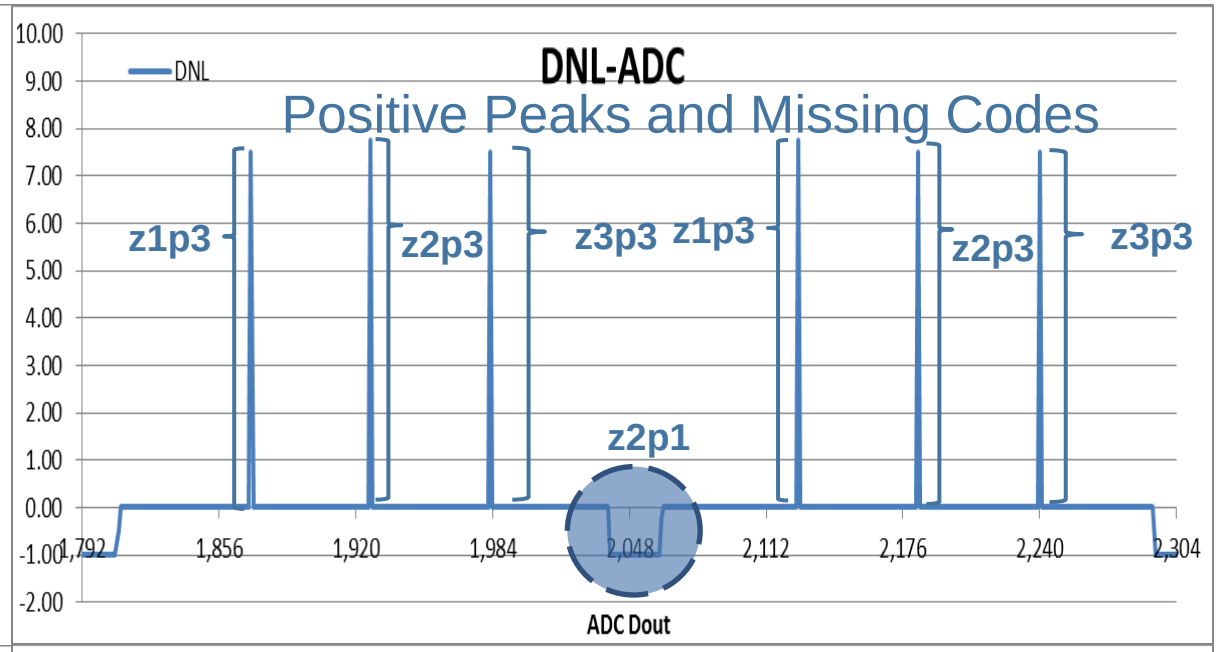
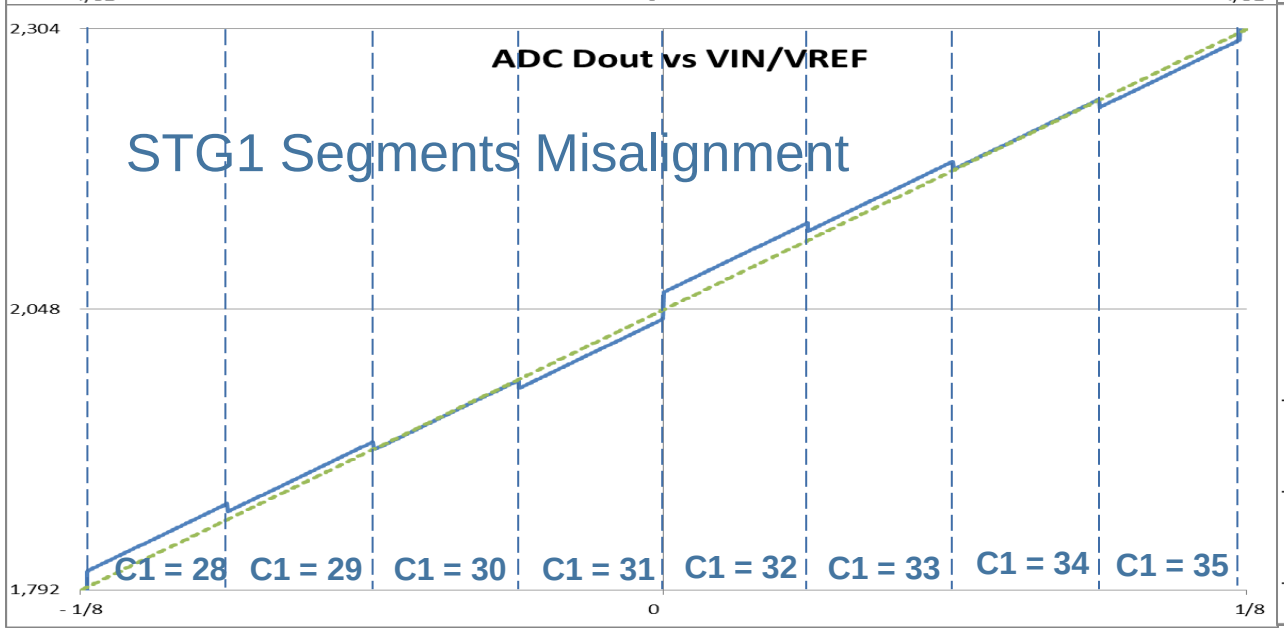
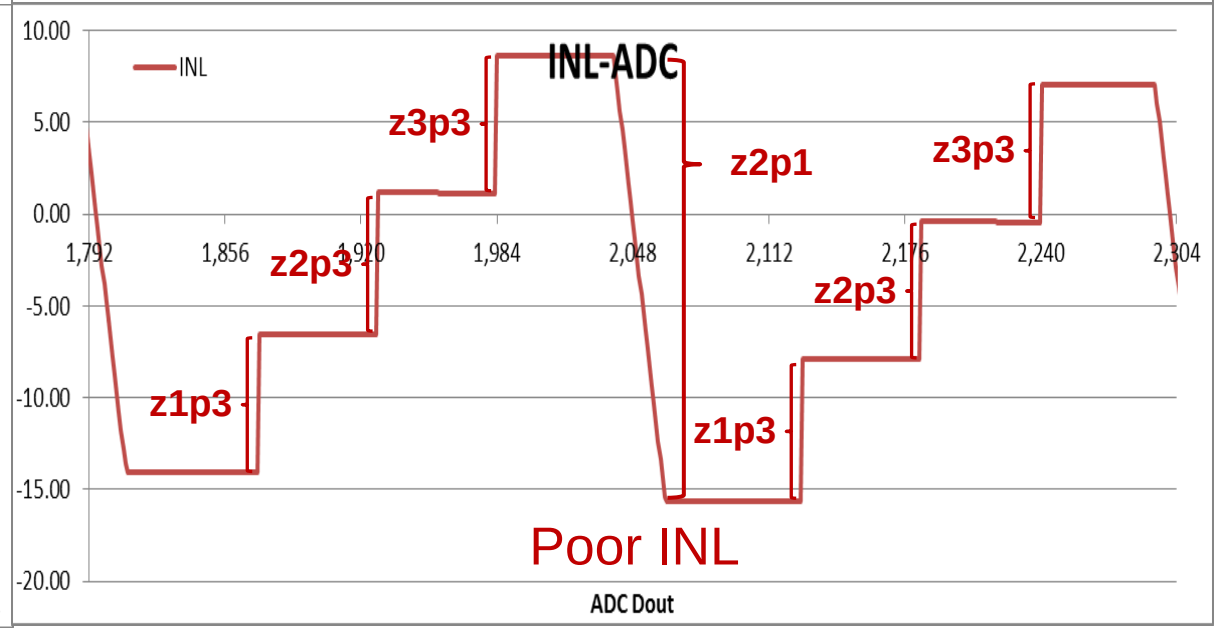
EFFECT OF THE STG1 DAC CAPACITORS MISMATCH ON THE ADC LINEARITY (6-BIT STG1)









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Send us your questions.
We are glad to help you.
Thank you!