Radiation Hardening by Design Concepts for 7-nm FinFET Technologies

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Outline

- A few words about imec and DARE radhard platforms
- Motivation for 7-nm technology study
- The INFINIT project
- Test vehicles
- Design concepts
- Test plans
- Conclusions

Existing RadHard IP & Design platforms

Design Against Radiation Effects (DARE)

DARE180U

- UMC 180nm Mixed-Mode RF 1.8V / 3.3V
- SEL LETth > 60 MeV.cm^2/mg
- SEU FF (HIT)
- TID tolerance > 1 Mrad(SiO_2)
- -55°C ~ 125°C
- Gate density = 25 kgates/mm^2
- Single & dual port memory compilers

DARE65T

- TSMC 65nm Low-Power Mixed-Mode RF 1.2V / 2.5V
- SEL LETth > 70 MeV.cm^2/mg
- SEU FF (DICE)
- TID tolerance > 100 krad(SiO_2)
- -40°C ~ 125°C
- Gate density = 250 kgates/mm^2
- Single port memory compiler / 5 dual port memories

DARE180X

- XFAB 180nm 1.8V / 3.3V
- SEL LETth > 60 MeV.cm^2/mg
- SEU FF (DICE)
- TID tolerance > 100 krad(SiO_2)
- -40°C ~ 125°C
- Gate density = 50 kgates/mm^2
- 5 dual port memories

DARE22G

- GF 22nm FDSOI 0.8V / 1.8V
- SEL LETth > 70 MeV.cm^2/mg
- SEU FF (DICE)
- TID tolerance > 100 krad(SiO_2)
- -40°C ~ 125°C
- Gate density = 2.5 Mgates/mm^2

RadHard IP & Design services

Which mitigation approaches are available for 7-nm FinFET?

DARE Platforms

- Radhard solution using standard commercial technology
- Digital and analog design flows
- Supported by ESA, European Commission, and in cooperation with CERN
- Various foundry technologies
  TSMC, UMC, XFAB, GF
- From 180nm down to 22nm and below
- Flexible towards application needs

DARE Mitigation Approach

- Guard rings to kill latch-up
- Single-event-upset hardened flip-flops
- Single-event-transient hardened clock tree cells
- Single-event-upset & transient hardened memories
- Enhanced physical implementation flow with extra checks
- Single-event-transient analog simulation flow
- Enclosed-layout-transistor for high total-ionizing-dose applications

https://www.imeciclink.com/en/asic-services/asic-design/dare

Why 7 nm?

Performance
- ☑ Smaller delays per cell
- ☒ RHBD must be compatible with the tough rules of the design flow
- ☒ Parasitic R and C

Power
- ☑ Power efficiency
- ☒ RHBD requires additional power
- ☒ Clock-gating cells must be fault-tolerant

Area
- ☑ Higher elements density
- ☒ Complicated design rules

Cost
- ☑ High demand of communication, automotive and AI chips
- ☒ High manufacturing price
- ☒ Small space-related market

Radiation hardness
- ☑ Local minimum in Alpha SER/bit
- ☑ Promising results for some FPGAs and test vehicles
- ☒ The critical energies/charges are extremely low
- ☒ The hardness assurance procedures require taking into account the process-related features

Space Applications of 7-nm FinFET Technology

From low- to high-volume production and small time to market

SiPs and chiplet technology are the drivers for the paradigm shift

GTE3-102ED - Interface and System-in-Package Technology

20ME – Under preparation

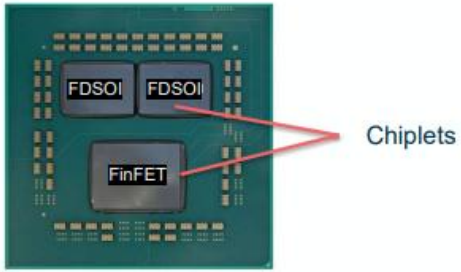
Description :

Contribute to the FPGA Development Roadmap

FinFET TSMC N7

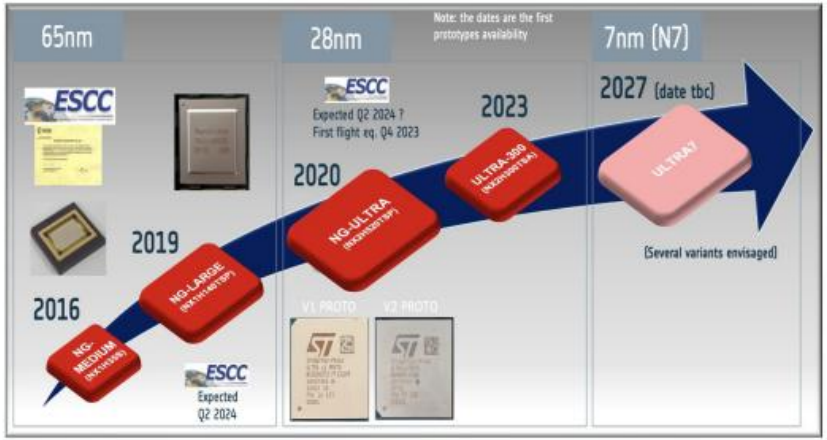
- Foundation library
- Die to die interface in 7nm
- HSSL LR 112G
- PCIe, Ethernet and SpF controller
- DDR4
- **FPGA/DSA chiplet**

SiP Technology



Roadmap: Field Programmable Gate Array (FPGA):

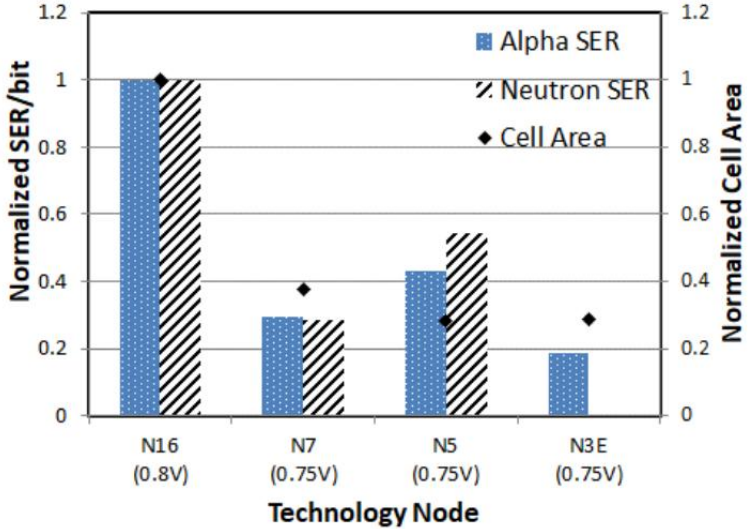
- Increase portfolio of European FPGAs (RF and security)
- Develop next generation FPGA ULTRA 7
- Mature FPGA development tools



From: Boris Glass, "EEE Space Component Sovereignty for Europe Ultra Deep Submicron Microelectronic Technologies". TEC-EDM 2024

Some 7-nm Process Features Affecting the Radiation Sensitivity

- Local minimum in Alpha SER/bit
- Proximity of high-Z materials to the active volume
- Possible enhanced layout sensitivity due to the mechanical stress dependence
- Possible channel stop (anti-punchthrough) doping layers
- No details on metal stack available for designers
- Complex layer usage for the gates
- Usage of Si_3N_4 (possible (EL)DRS effects)

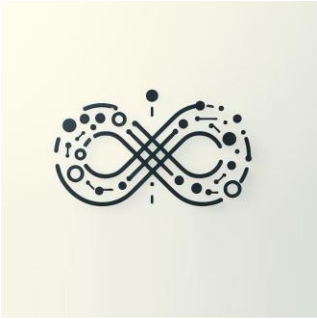


Normalized scaling trends in the per-bit alpha and neutron SER of SRAMs as a function of FinFET technology nodes

B. Narasimham, et al., "Scaling Trends and Bias Dependence of SRAM SER from 16-nm to 3-nm FinFET," in 2024 IEEE International Reliability Physics Symposium (IRPS)

INFINIT

Irradiation Assessment of N7 FinFET Technology for Innovative Digital Telecom Applications



- The main objective:
  - To gain a deep understanding of the N7 FinFET process technology for use in digital space applications
- Two sub objectives:
  - Create a minimum set of hardened standard cells
  - Establish a standardized radiation evaluation test vehicle approach for fast(er) evaluation of new advanced process technologies

- Challenges
  - **INFINIT** is a pre-cursor project for the **ESA UDSM** programme. Further projects depend heavily on the outcome of **INFINIT**. Therefore, timely presentation of final results as well as having a baseline radiation-hard library is of utmost importance for further success of the N7 technology implementation in near-future space projects.

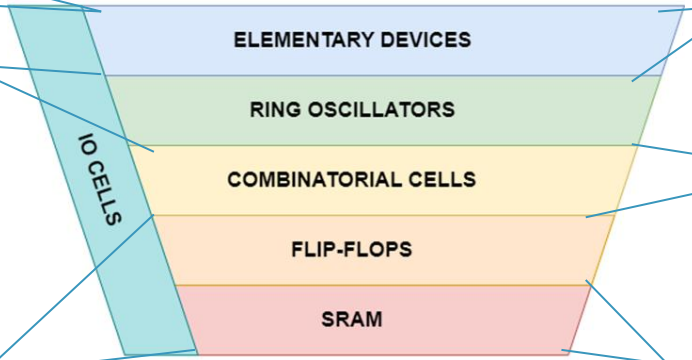
https://connectivity.esa.int/projects/infinit

Test Vehicle: Hierarchical Approach

The representative cells from the foundry, a library vendor and imec

- **FinFETs:**
  - Geometry variation: # of fins, gate pitch, L (channel length)
  - Vt flavors
  - Core and IO

- **Resistors**
- **BJTs**



- **INV**
  - Drive strengths from 2 to 24
  - 300-nm and 240-nm height
- **INV** with SET filters
- **Majority Voters**
- **Combinatorial cells** from the tests are used in the clock tree

- **INVs** with the same FinFETs as in the FinFET block

- Regular
- **DICE** (with and w/o built-in tap-cells)
- **TMR DFF**
- **Multi-bit DFF**: regular 2-bit, and 2-bit TMR

- The most process-representative block:
  - Highest element density
  - Single- (2 types of bit cells) and Dual-port
  - Vt flavors for control and readout circuits
  - Standard memory compilers

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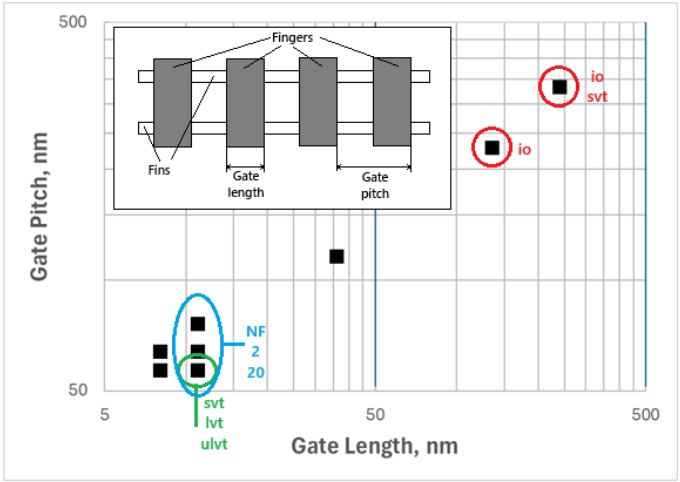
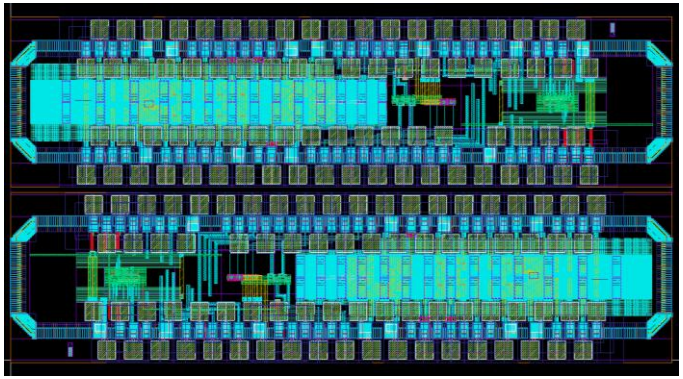
Radiation Effects Test Vehicle Analog (RETVA)

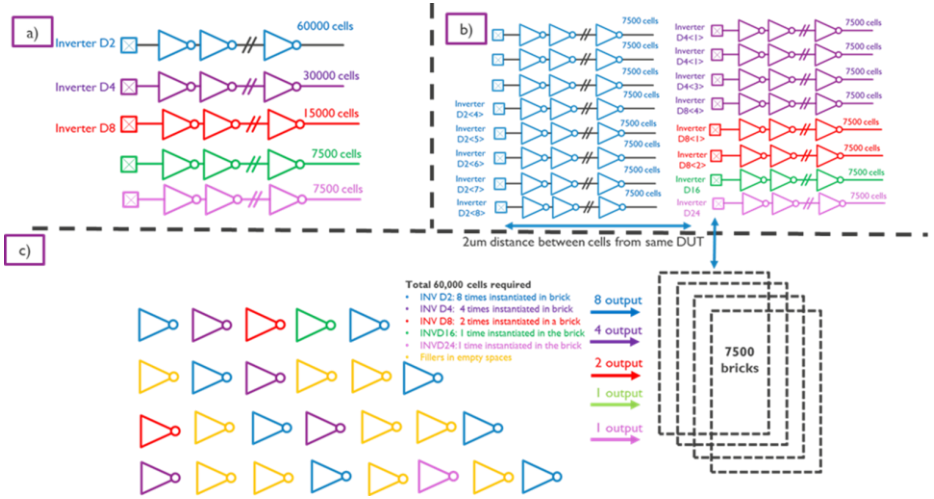
- 2 mm^2 chip (wire-bonded)
- Duplicated (for ESD tests and on-chip probe testing)
- Devices (Blocks) Under Test:
  - FinFETs
  - Resistors
  - BJTs
  - Ring Oscillators
  - ESD diode

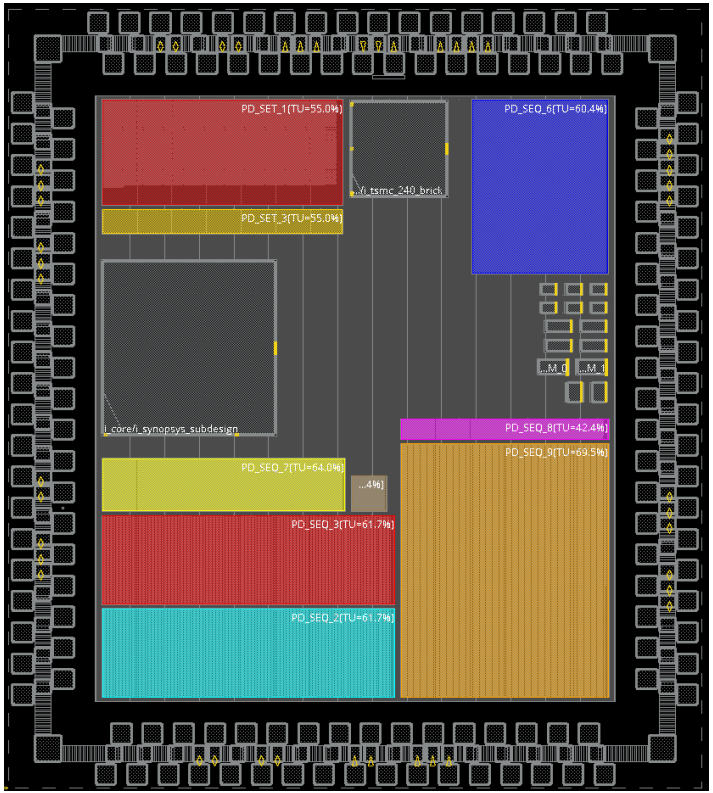




Radiation Effects Test Vehicle Digital (RETVD)

- 2x2.7 mm^2 chip (wire-bonded)
- SRAM blocks
- SEU test structures (shift registers)
- SET test structures (inverter chains) as bricks:





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Major Design Concepts

Applicable to FinFETs

Internal spatial redundancy (DICE, LEAP, STG, etc.)

- Sensitive volumes must be placed at a minimal distance or in a special way minimizing collected charge
- Complicated layout, huge effects of parasitics

Local, distributed, global, block Triple Modular Redundancy

- Usually made by means of scripts
- The needed "safe" distance is unknown
- The delays differ from one copy to another (a kind of skew)

Temporal redundancy (C-elements-based designs)

- Critical delay time is yet unknown

Critical distance estimation

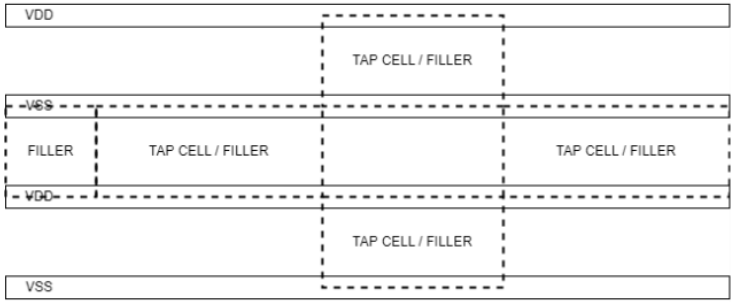
- We don't know the charge collection distance for the used technology yet
- A test SRAM block with small bit cells can be used as a kind of "image sensor"
- In the absence of 7 nm FinFET SRAM SEU error maps for the present moment, we can use the critical distances from the published results for 5-nm FinFET as the reference ones, assuming that the charge sharing mechanism does not change drastically from 7-nm to 5-nm node
- The critical separation distance d_{crit} is estimated as ~0.76 µm
- It is much less than the reported ones for 90 nm and 65 nm bulk CMOS, however, it is consistent with the experimental results for 16 nm FinFET presented, where the average sensitive node separation distance was about 1 µm, which allowed reaching the threshold LET above 30 MeV×cm^2/mg
- For the references, please see the full paper

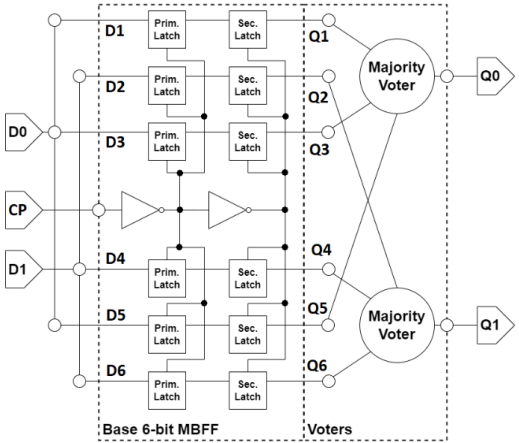
Simulation results

Description	Vendor	Total Area (n.u.)	Average Delay (n.u.)	Average Power per bit (n.u.)
STANDARD	FOUNDRY	1.00	1.00	1.00
STANDARD 2-BIT	FOUNDRY	1.95	1.09	1.2
STANDARD 6-BIT	FOUNDRY	5.48	1.52	1.89
2-BIT TMR	IMEC	8.12	1.05	6.26
DICE	IMEC	3.87	1.13	2.11

- DICE cell design is based on 65-nm placement concept
  - "Unused" area, which is with tap-cells (option 1) and fillers (option 2)
  - 3-row, wide design
- Multi-bit flip-flops are used in
  - optimized timing
  - two 12-transistor majority voters are built into the cell
  - 6 rows (the height of each row is 300 nm)

The layout plan for DICE DFF with tap- or filler cells:





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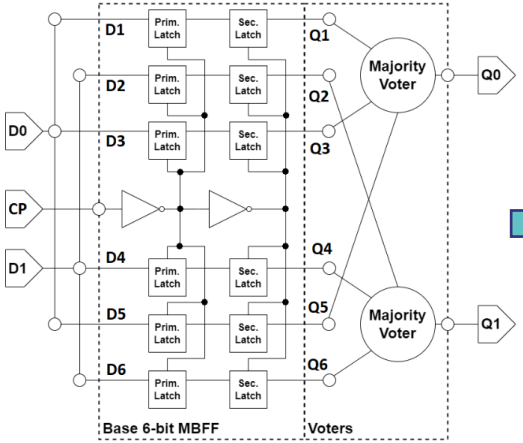
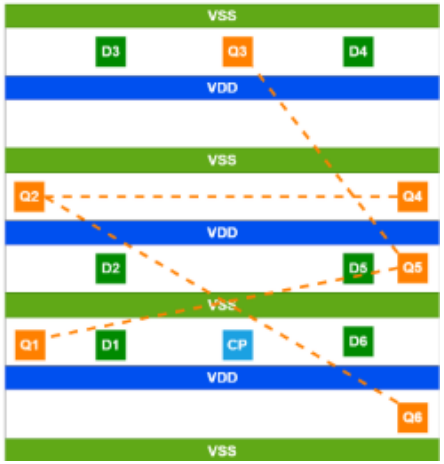
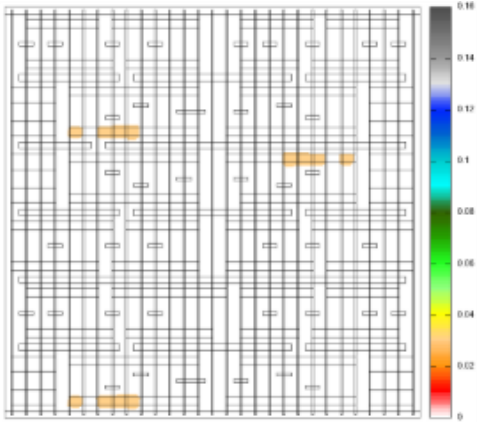
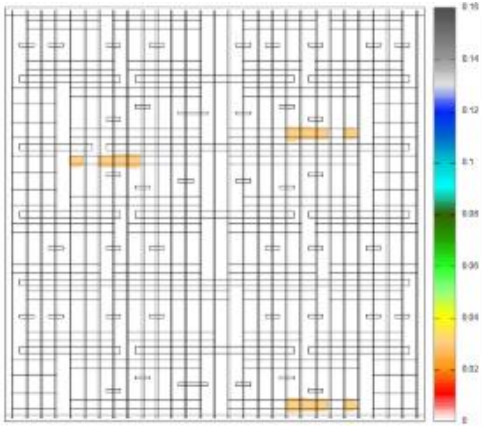
How to ensure the proper placing/connecting in multi-bit DFFs?

TFIT









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“Penalties” comparison with 3-nm FinFET

Yoni Xiong, et al., IEEE TNS, 2025

TABLE I
RHBD DESIGN OVERVIEW

TYPE	DESIGN NAME	DESCRIPTION
Temporal	(a) Guard Gate (GG)	Usage of C-element to compare a signal and its delayed copy
Temporal/ Hysteresis	(b) Schmitt-Trigger (ST)	Increase switching voltage with hysteresis on the output node
Redundancy/ Spatial	(c) Dual Interlocked Storage Cell (DICE)	Latch design with duplicated circuit nodes
Spatial Sampling	(d) Triple Modular Redundancy (TMR)	Triplication of storage elements with a majority voter at the output

TABLE II
COMPARISON OF AREA, POWER, AND SPEED OF VARIOUS RHBD FF DESIGNS, (RELATIVE TO D-FF)

DESIGN NAME	AREA	# OF TRANSISTORS	CLOCK-TO-Q*
D-FF	1.00	1.00	1.00
GG-FF	1.23	1.42	1.55
ST-FF	1.35	1.67	1.65
DICE-FF1	2.00	2.08	1.20
DICE-FF2	5.45	2.08	1.20
TMR-FF	5.45	3.58	1.30
LEAP-FF1	2.00	2.58	1.20
LEAP-FF2	2.91	4.92	1.40
LEAP-FF3	3.64	5.38	1.40

*Clock-to-Q simulations were done on the schematic level

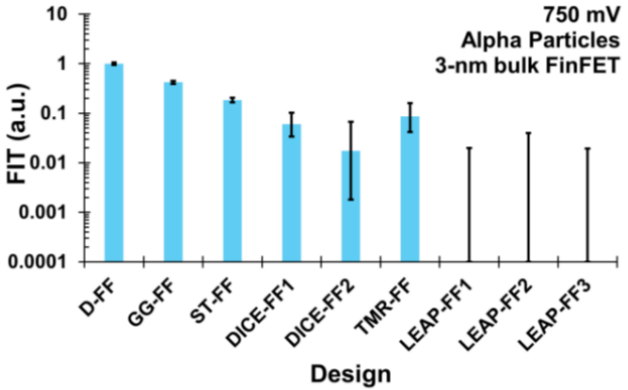

Fig. 3. Comparison of alpha FIT across eight RHBD FF designs. All FITs are normalized to those of the D-FF at 750 mV and for alpha particle exposures.

Description	Vendor	Total Area (n.u.)	Average Delay (n.u.)	Average Power per bit (n.u.)
STANDARD	FOUNDRY	1.00	1.00	1.00
STANDARD 2-BIT	FOUNDRY	1.95	1.09	1.2
STANDARD 6-BIT	FOUNDRY	5.48	1.52	1.89
2-BIT TMR	IMEC	8.12	1.05	6.26
DICE	IMEC	3.87	1.13	2.11

Area per bit: 4.06

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Test plans for Total Ionizing Dose (TID) Effects

RETVA			RETVD		
Dose Rate	Source	Irradiation conditions	Dose Rate	Source	Irradiation conditions
Low (LDR) < 0.1 rad(Si)/s	Co-60	• Room T • VDD+10%	Standard (SDR) ~ 1 rad(Si)/s	Co-60	• Room T • VDD+10%
Standard (SDR) ~ 1 rad(Si)/s	Co-60	• Room T • VDD+10%			

Test plans for Single Event Effects (SEE)

RETVA			RETVD		
Effect	Source	Irradiation conditions	Effect	Source	Irradiation conditions
Single Event Latchup (in case of SEL registration in RETVD)	SPA/TPA Laser	• Room T • VDD+10%	Single Event Latchup	HIF (heavy ion facility)	• High T • VDD+10%
			Single Event Upsets Single Event Transients	HIF HEP (high energy protons) SPA/TPA Laser	• Room T • VDD (VDD-10%)

Conclusions

- We present the design concepts of the Single Event Upset (SEU) hardened D-flip-flops (DFF) for 7-nm FinFET technology
- The parameters of DICE, 2-bit TMR DFF (designed from the standard 6-bit one) and single-bit TMR DFFs are compared with those of the standard single-bit and 6-bit DFFs
- The nodal separation in DICE cell leads to 13% loss in the speed, which is comparable with 15% loss in area-minimized DICE solution without separation reported in literature
- For 2-bit TMR DFF, the performance degradation is lower than for DICE DFF, while the SEU sensitivity is at least comparable due to the sensitive node separation
- The average power per bit is about 3 times higher for 2-bit TMR DFF compared to 1-bit of the standard 6-bit DFF. The average delay is comparable with that of standard 2-bit DFF

Thank you for your attention!

https://www.imeciclink.com/en/asic-services/asic-design/dare

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