

Extreme-Environment ASIC Design for Scientific Instruments

Soumyajit Mandal

Brookhaven National Laboratory

June 16, 2025



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Overview

- Introduction
- Cryogenic multi-channel front-end ASICs for low-noise readout of charge or light signals
- Low-power data links for stitched pixel sensors
- An integrated negative bias voltage generator for stitched pixel sensors

Acknowledgements

Instrumentation Department

- Gabriella A. Carini
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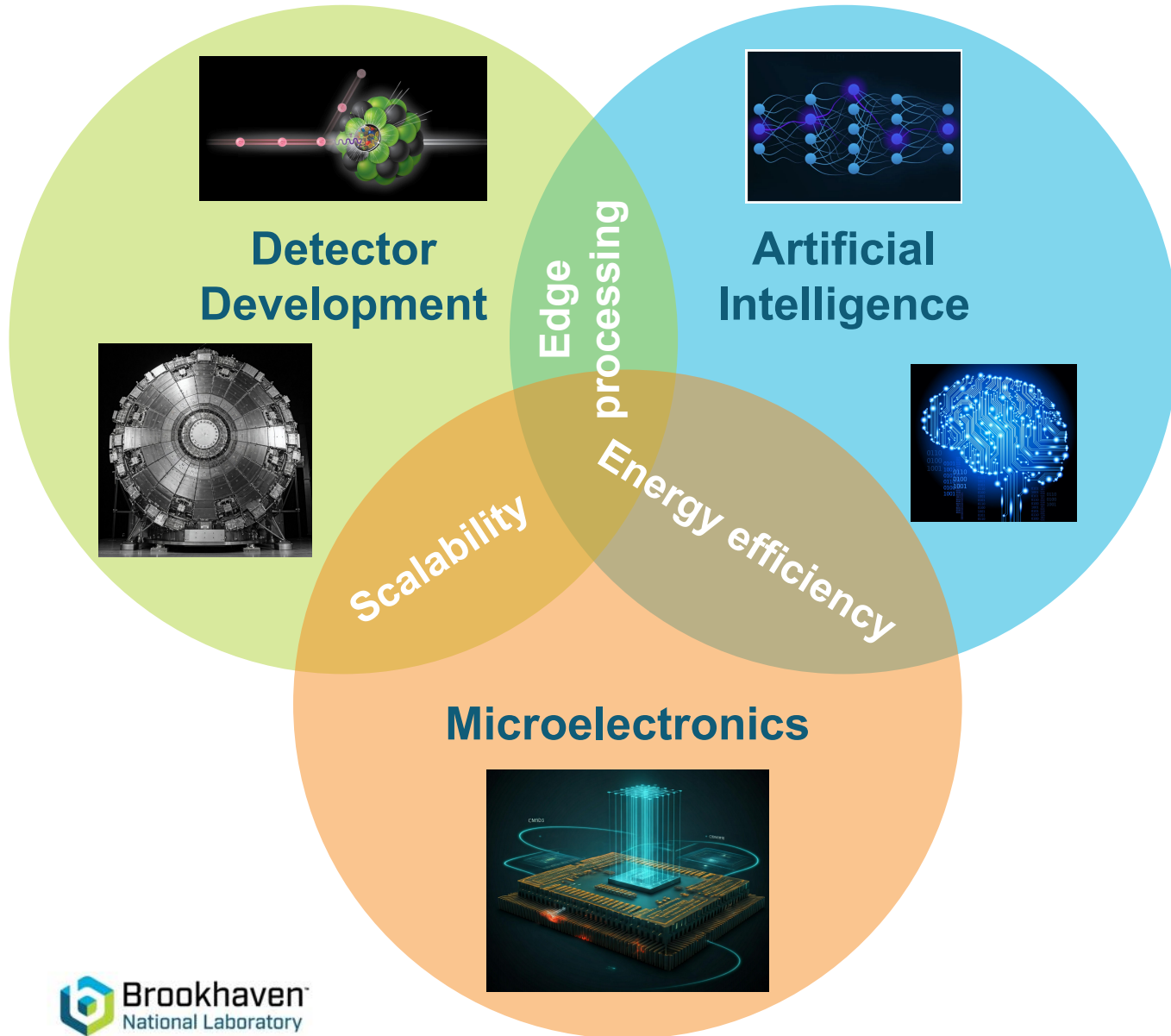
Physics Department

- Hucheng Chen
- Shanshan Gao
- Jay Hyun Jo
- Lingyun Ke
- Steven Kettel
- Xin Qian
- Vladimir Tishchenko
- Chao Zhang

Collaborators

- Iain Sedgwick (RAL)
- Amanda Krieger (LBNL)

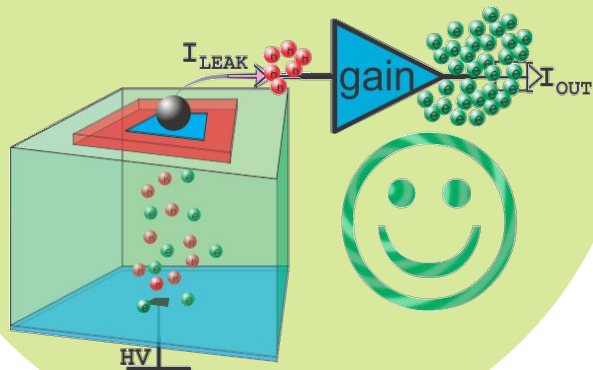
Overview



- ❑ This talk overviews our work that lies at the intersection of detector development, artificial intelligence, and microelectronics
- ❑ **As detectors evolve to produce increasing amounts of data, AI techniques that enable efficient edge data processing and extraction of information close to the data source are crucial in improving detector performance**
- ❑ Use of novel microelectronics technologies for energy-efficient readout and processing is being explored
- ❑ Concepts, frameworks and hardware developed are also applicable to scientific use cases beyond detectors

Team Expertise

Detector Development

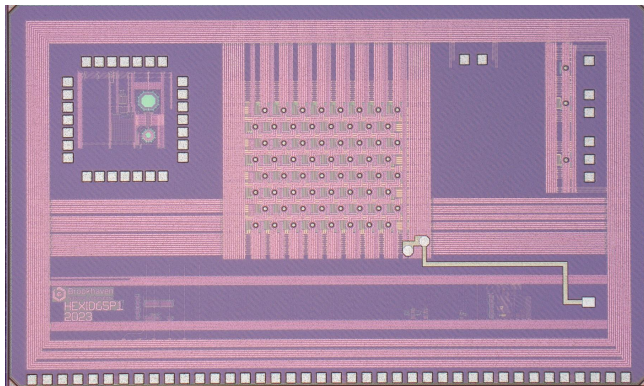


- ❑ **Instrumentation Department (IO)**
- ❑ **Design, characterization and testing of low-noise, low-power, large mixed-signal application specific integrated circuits (ASICs) for:**
 - ❑ Readout of detectors operating in extreme environments such as cryogenic temperatures and high-radiation (DUNE, nEXO)
 - ❑ Hybrid spectroscopic and imaging pixel-detectors for X-rays (BES, BER, NASA)
 - ❑ Monolithic active pixel sensor (MAPS) detectors (EIC, FCC)

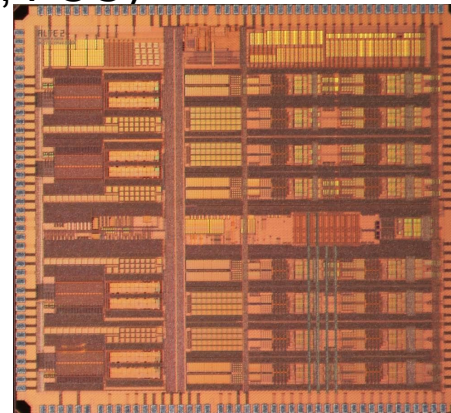


Functional prototypes showcase Brookhaven's innovation

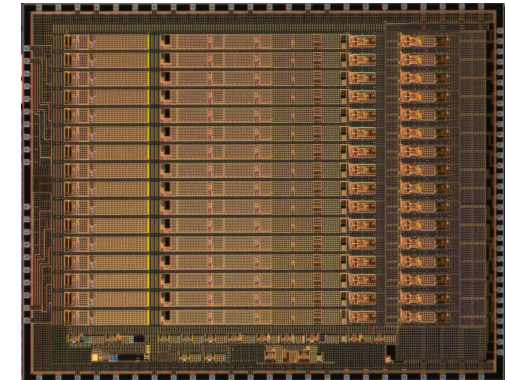
[At IEEE NSS/MIC/RTSD conference, Tampa, FL, 2024]



❑ HEXIDP1 65 nm



❑ ALFE2 130 nm



❑ LArASIC_P4 180 nm

Team Expertise (2)

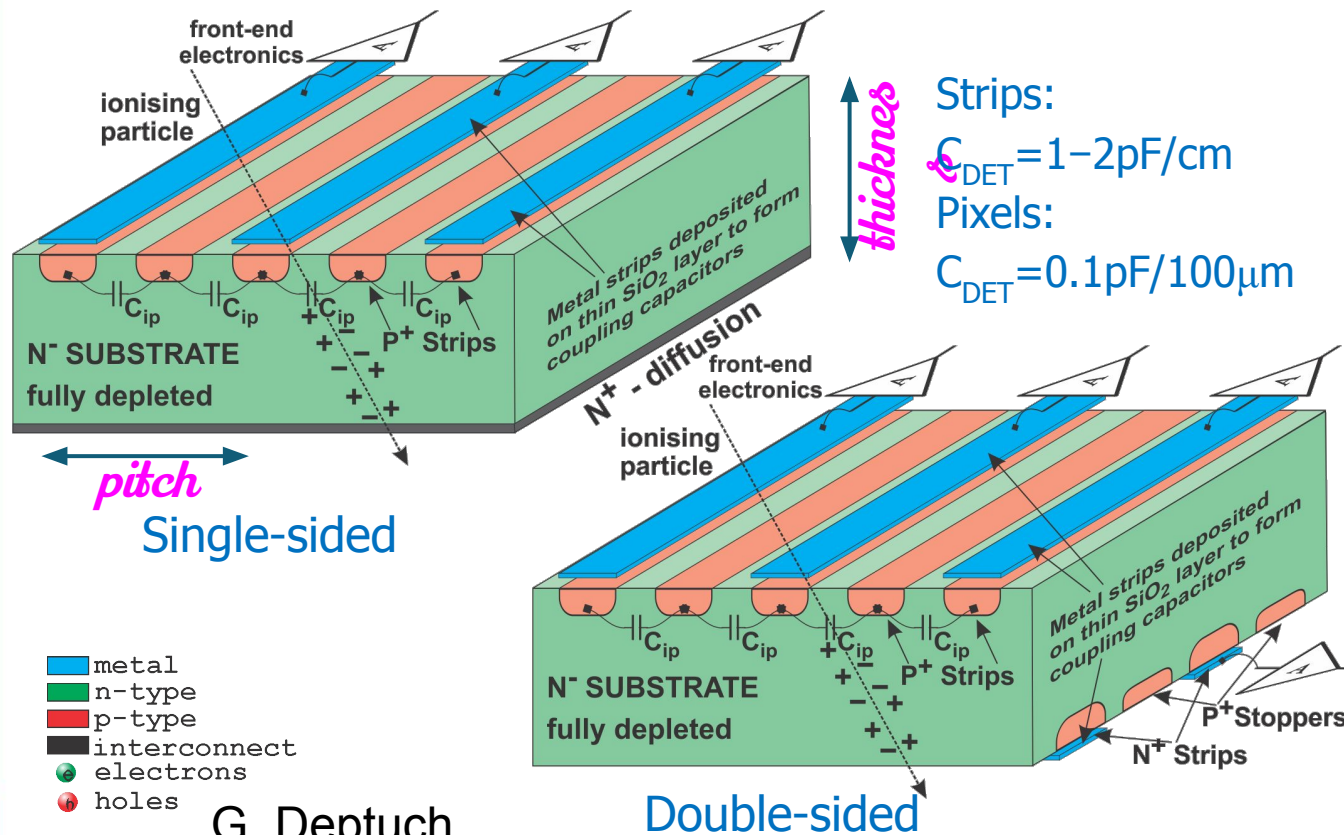
- Computing and Data Sciences (CDS) directorate
 - Accelerating computing and domain science by providing the technical expertise, compute and data resources, and research environment to drive scientific discovery
 - **Key areas:** Computational Research; Systems, Architectures, and Emerging Technologies; Scientific Computing and Data Facilities
- Center for Functional Nanomaterials (CFN)
 - Nanoscale Science Research Center operated for the U.S. Department of Energy (DOE) at BNL
 - Focused on developing nanomaterial synthesis-by-assembly methods and realizing functional material designs from polymer, nanoparticle, biomolecule-based, and 2D material components.
- National Synchrotron Light Source-II (NSLS-II)
 - One of the world's newest, most advanced synchrotron light sources
 - Enables study of materials with nanoscale resolution and exquisite sensitivity by providing cutting-edge X-ray capabilities



Geometries of Solid-State Sensors

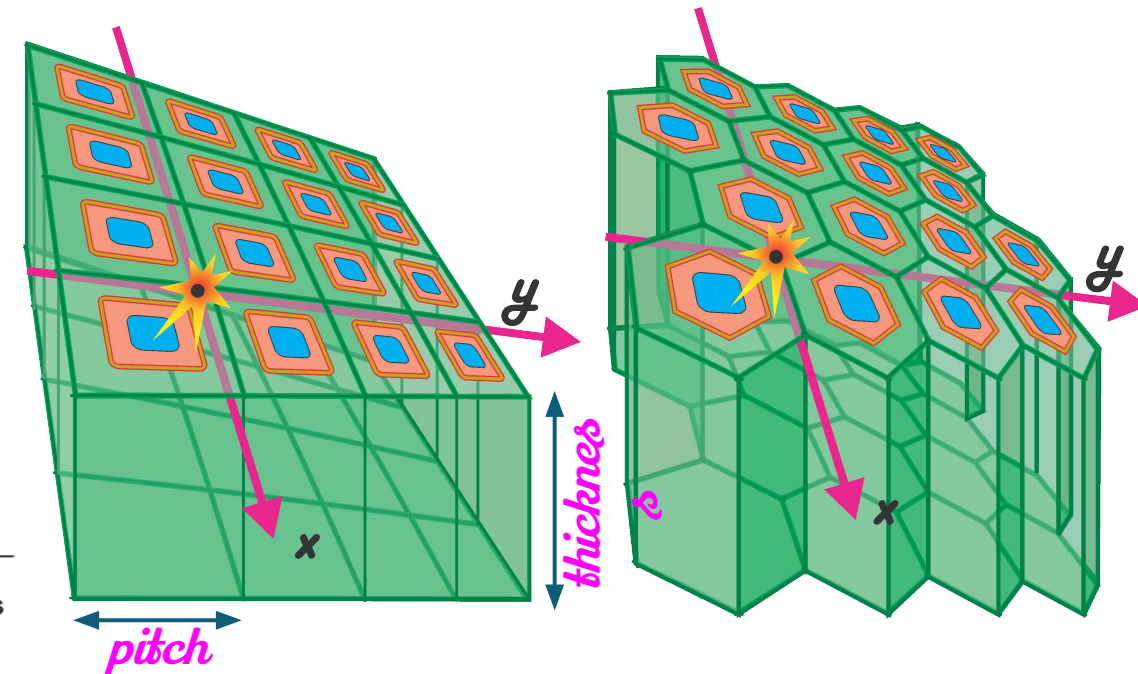
STRIPS

Strips sensors deliver 1D - (sometimes 2D – but prone to ambiguity) aware information about incident radiation



PIXELS

Pixel sensors deliver 2D - (sometimes 3D) aware information about incident radiation



Square (rectangular)

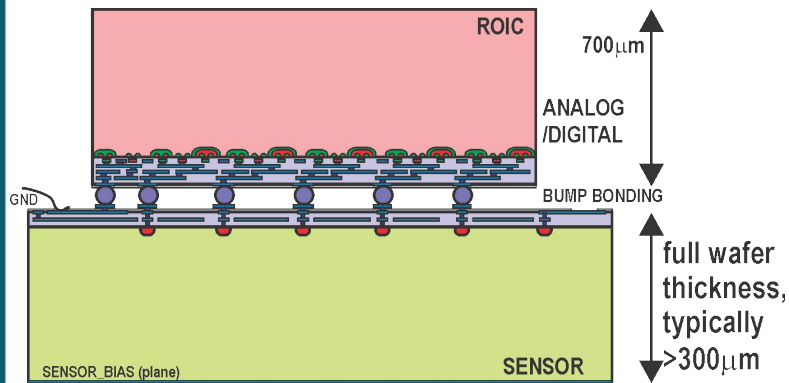
Hexagonal

Both types of sensors may be used to measure time of arrival

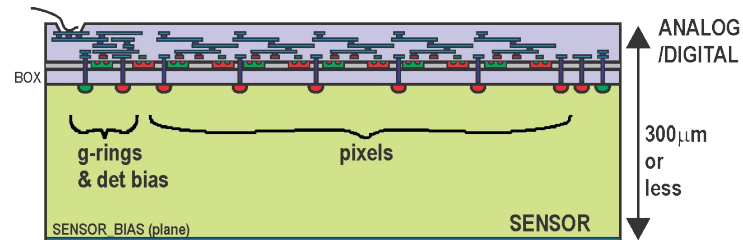
Types of pixel detectors

Three types of physical integration of pixel detectors

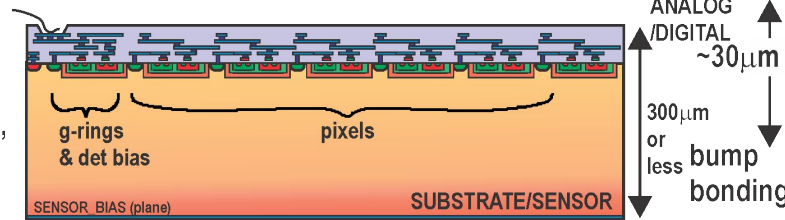
Hybrid



Monolithic

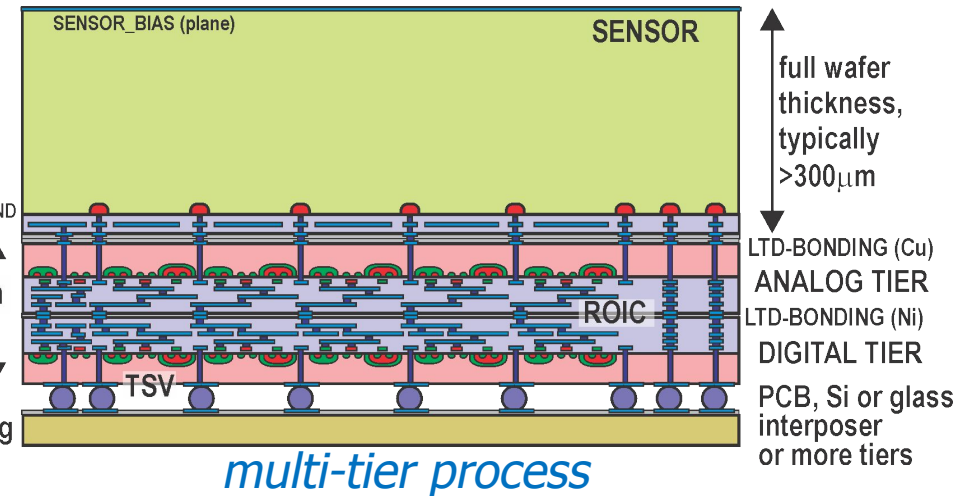


SOI process



bulk process

3D integrated



multi-tier process

Use of ASICs within detectors

High-Energy Physics

CMS DETECTOR

Total weight : 14,000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T

STEEL RETURN YOKE
12,500 tonnes

SILICON TRACKERS
Pixel ($100 \times 150 \mu\text{m}$) $\sim 1\text{ m}^2 \sim 66\text{ M ch.}$
Microstrips ($80 \times 180 \mu\text{m}$) $\sim 200\text{ m}^2$

SUPERCONDUCTING SOLENOID
Niobium titanium coil carrying $\sim 18,000\text{ A}$

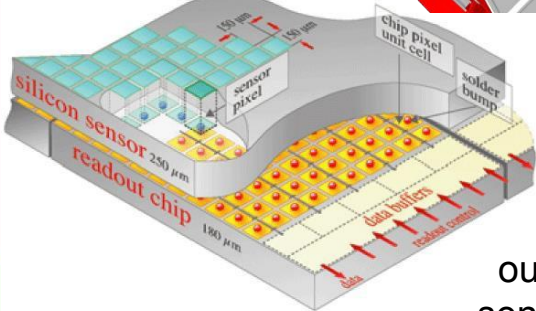
MUON CHAMBERS
Barrel: 250 Drift Tube, 480 Resistive Plate Chambers
Endcaps: 540 Cathode Strip, 576 Resistive Plate Chambers

PRESHOWER
Silicon strips $\sim 16\text{ m}^2 \sim 137,000$ channels

FORWARD CALORIMETER
Steel + Quartz fibres $\sim 2,000$ Channels

CRYSTAL
ELECTROMAGNETIC
CALORIMETER (ECAL)
 $\sim 76,000$ scintillating PbWO_4 crystals

HADRON CALORIMETER (HCAL)
Brass + Plastic scintillator $\sim 7,000$ channels



CMS (CERN)

<https://cms.cern/detector/identifying-tracks/silicon-pixels>

Readout channels are laid out in 2D matrix connected to sensor elements at same pitch

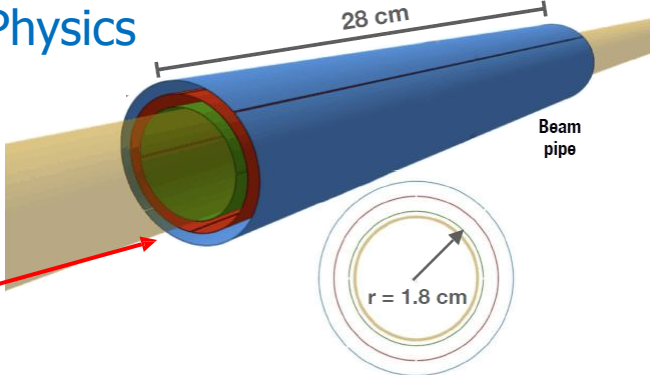
SILICON TRACKERS

Pixel ($100 \times 150 \text{ mm}^2$) $\sim 1 \text{ m}^2 \sim 66 \text{ M ch.}$

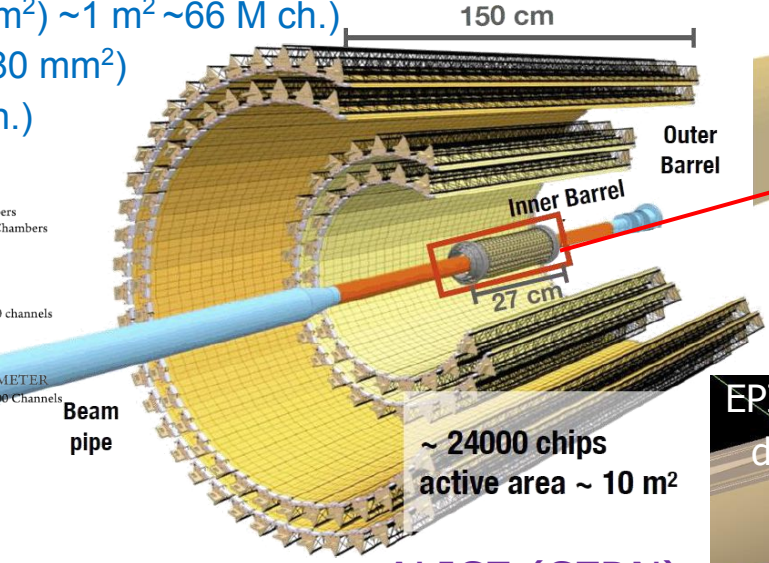
Microstrips ($80 \times 180 \text{ mm}^2$)

$\sim 200 \text{ m}^2 \sim 9.6 \text{ M ch.}$

Nuclear Physics



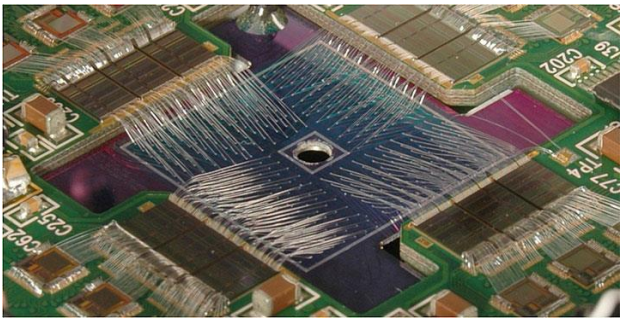
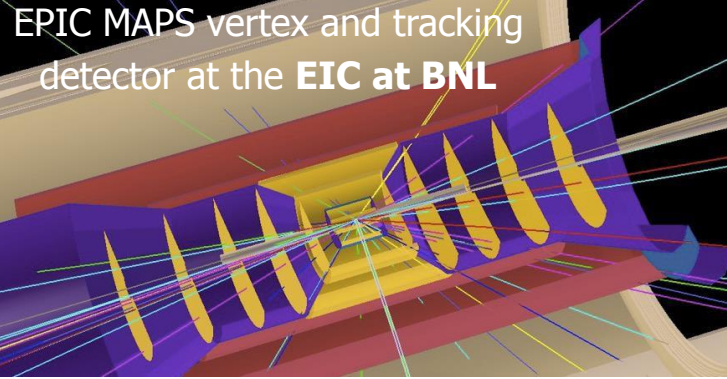
Si literally wrapped around finger



ALICE (CERN)

Astrophysics,
Photon Science (X-ray detection)

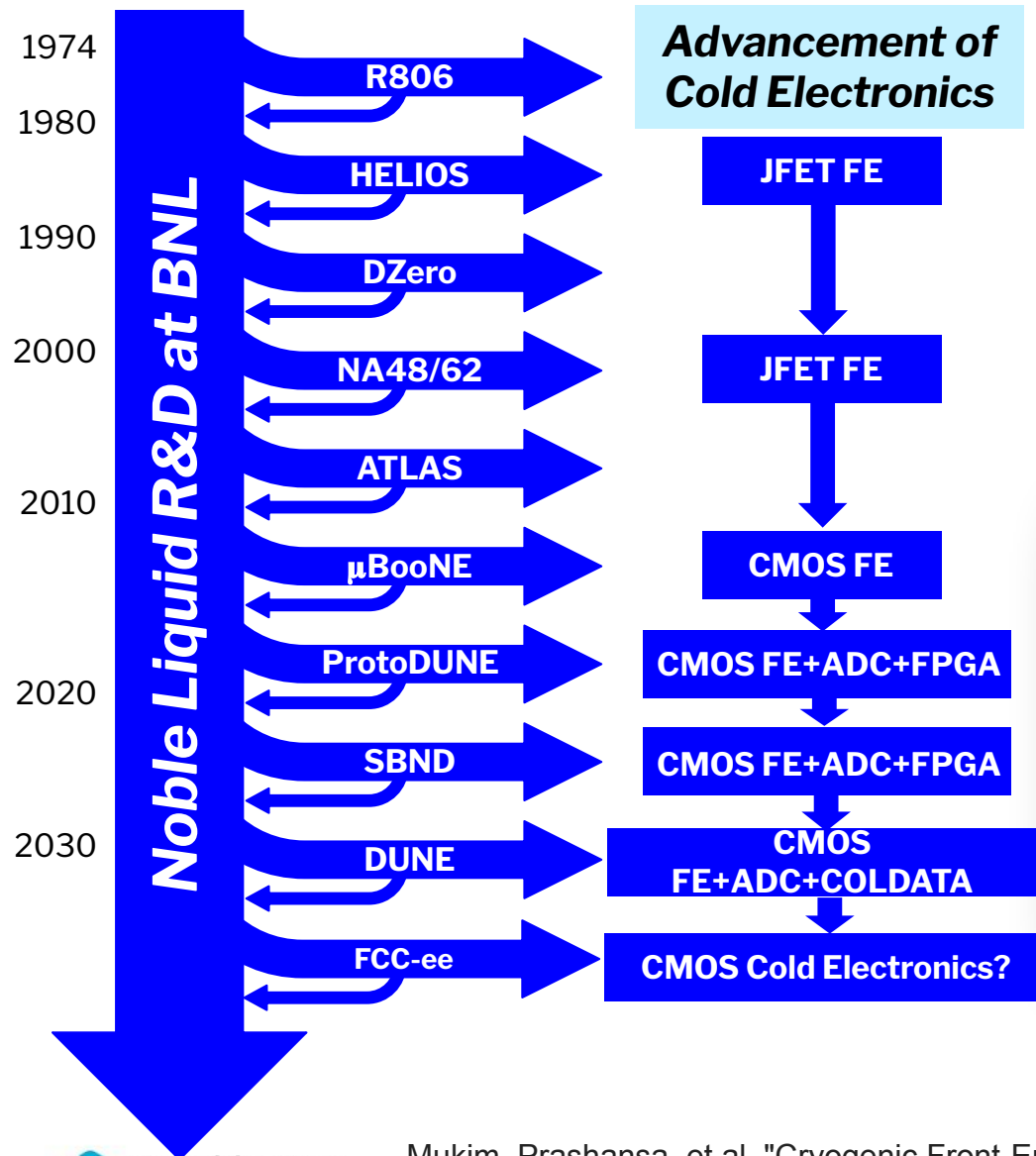
EPIC MAPS vertex and tracking
detector at the EIC at BNL



MAIA 20x20 (BNL)

Cryogenic Front-End ASICs for Low-Noise Readout of Charge or Light Signals

Long History of Noble Liquid Detector R&D at BNL



- BNL pioneered Liquid Argon (LAr) based detector technology in 1974
- **Readout electronics** has always been an **integral** part of detector R&D effort for **precision measurements** with noble liquid detectors

NUCLEAR INSTRUMENTS AND METHODS 120 (1974) 221-236; © NORTH-HOLLAND PUBLISHING CO.

LIQUID-ARGON IONIZATION CHAMBERS AS TOTAL-ABSORPTION DETECTORS*

W. J. WILLIS†

Department of Physics, Yale University, New Haven, Connecticut 06520, U.S.A.

and

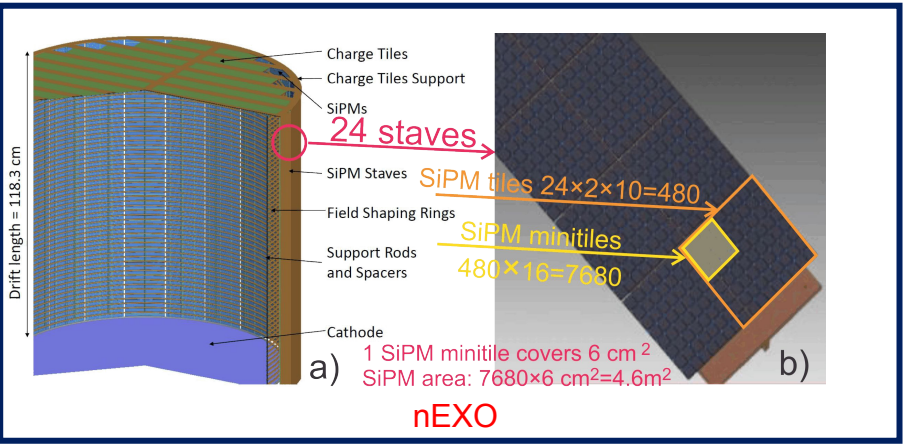
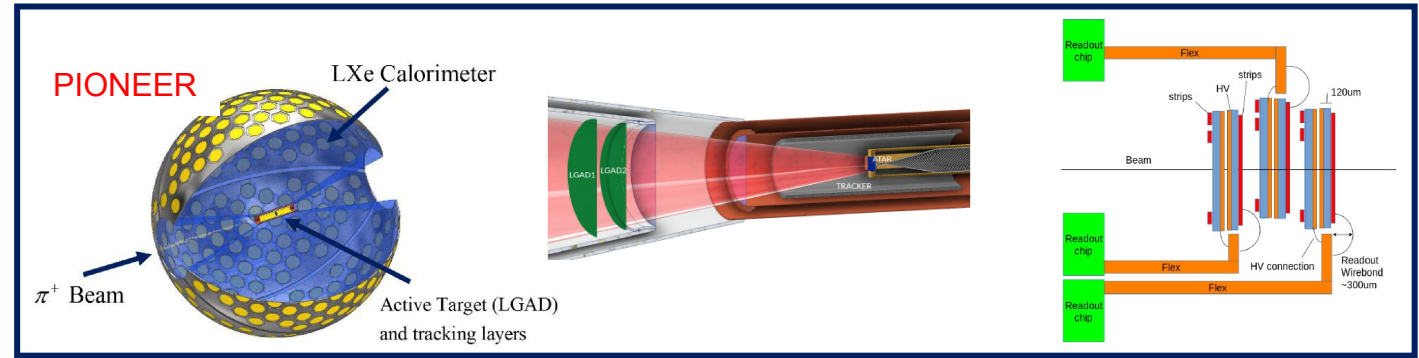
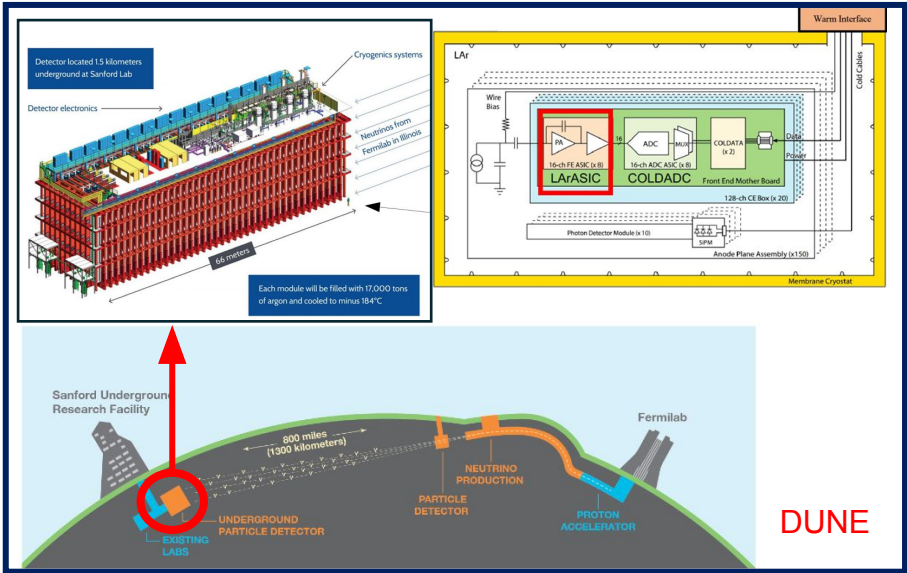
V. RADEKA

Instrumentation Division, Brookhaven National Laboratory, Upton, New York 11973, U.S.A.

Received 14 May 1974

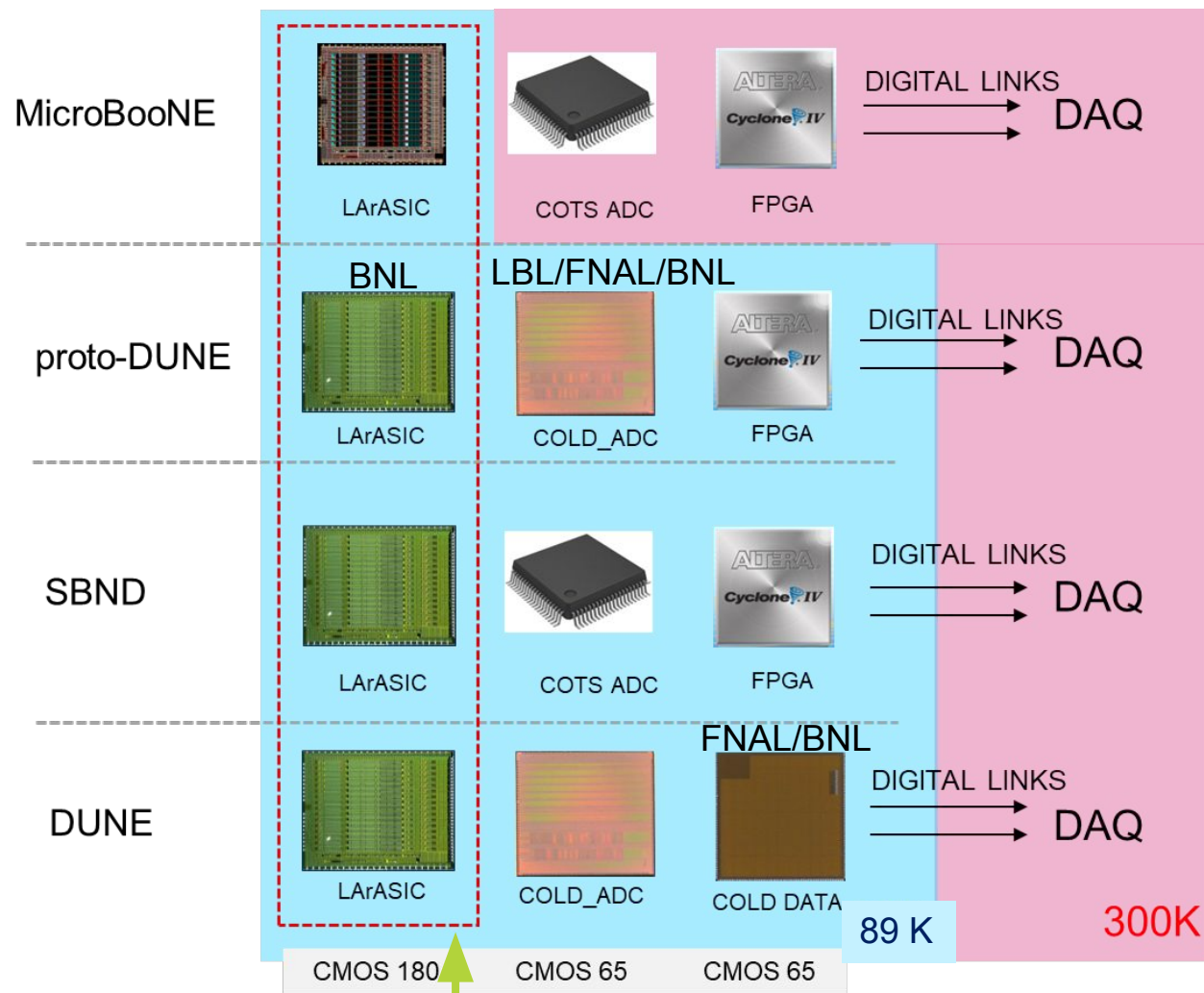
Applications of cryogenic front-end ASICs

Experiment	Temperature	Detector capacitance	Shaping time	Input noise (ENC)	Dynamic range
DUNE FD 3/4 charge readout	89 K – 300 K	150 pF – 200 pF	250 ns – 2 μ s	500 e ⁻ at 87 K	10 bits
nEXO light readout	160 K – 300 K	5 nF	1 μ s	0.1 pe ⁻ at 160 K	10 bits
FCC-ee	TBD	TBD	< 250 ns	TBD	> 10 bits
PIONEER	160 K – 300 K	20 pF	20 ns	570 e ⁻ at 160 K	10 bits



Status of Cryogenic Front-end ASICs

About a decade of development



**Peaking time programmable
between 500 ns and 3 μ s**

3 ASICs vs. 1 ASIC solution:

- Initially two readout options were proposed:
 - 3 ASICs vs. 1 ASIC (idea of building 1 ASIC, combining FE/ADC/transmission brought in 2016 and included as parallel path of development)
- Evolutionary development MicroBooNE $\rightarrow$ DUNE led to the 3 ASIC solution that:
 - Helped perfect the FE (through multiple iterations)
 - Allowed debugging (procedure for ADC calibration)
 - Allowed independent optimization of each chip
 - Disallowed analog – digital interfaces

To meet the demands of next generation experiments $\rightarrow$ cryogenic front-end ASIC in a newer technology node - 65 nm

Currently in development: CHARMS250 (CHARge amplifier + Shaper $\rightarrow$ 65 nm cryogenic analog front-end ASIC with 250 ns shortest peaking time)

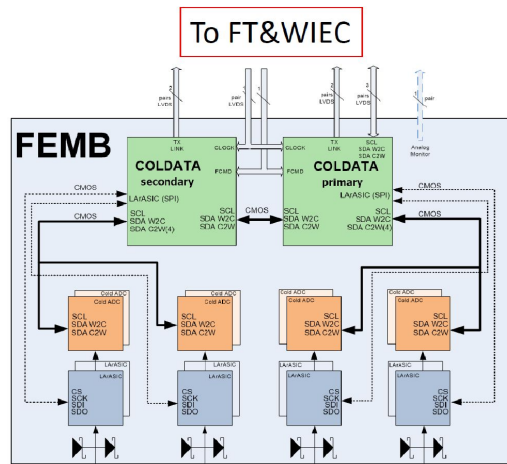
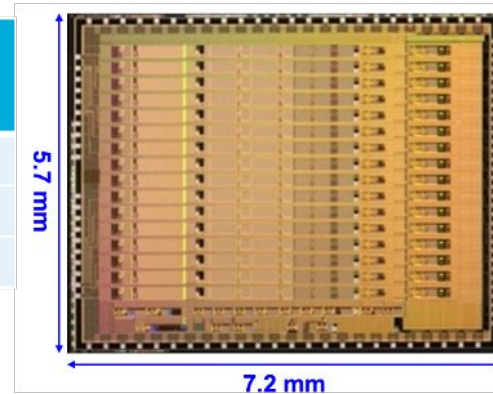
CHARMS10 with 10 ns shortest peaking time also planned for development

Status of LArASIC

LArASIC MPW met all the DUNE requirements → fabricated ~1800 P5 and 1800 P5B (180 nm) chips (engineering run) for ProtoDUNE II

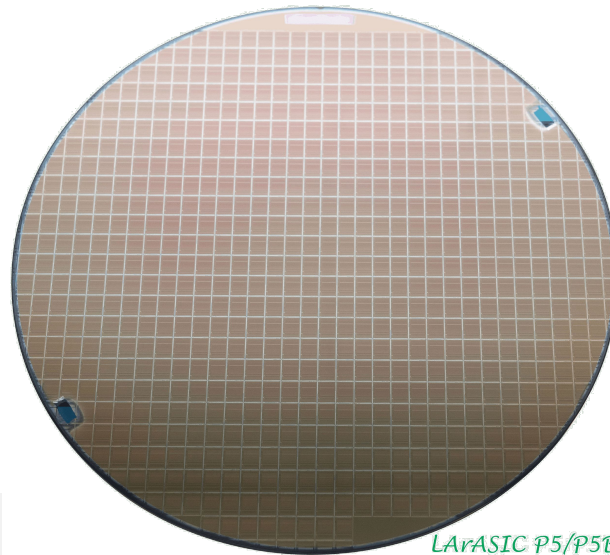
LArASIC Chips	Temp.	Tested Chips#	Good # (All channels are normal)	Yield
P5	RT	49	49	100 %
P5B	RT	1642	1635*	~99.57 %
P5B	LNT	317	317	100 %

P5B has improved input ESD protection compared to P5



128 CHs FROM Anode planes (APA or CRP)

24 FEMBs arrived at CERN for ProtoDUNE-II installation

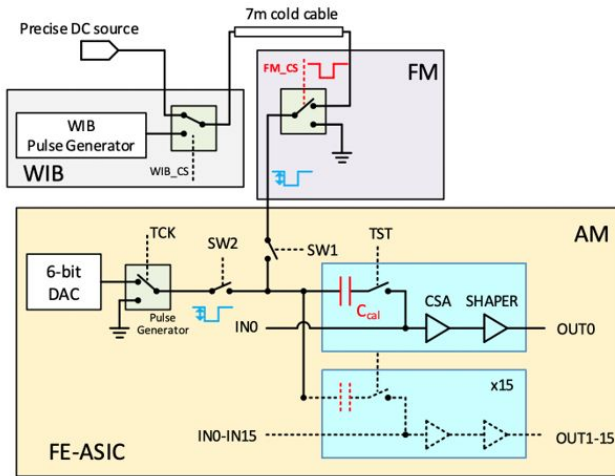


LArASIC P5/P5B

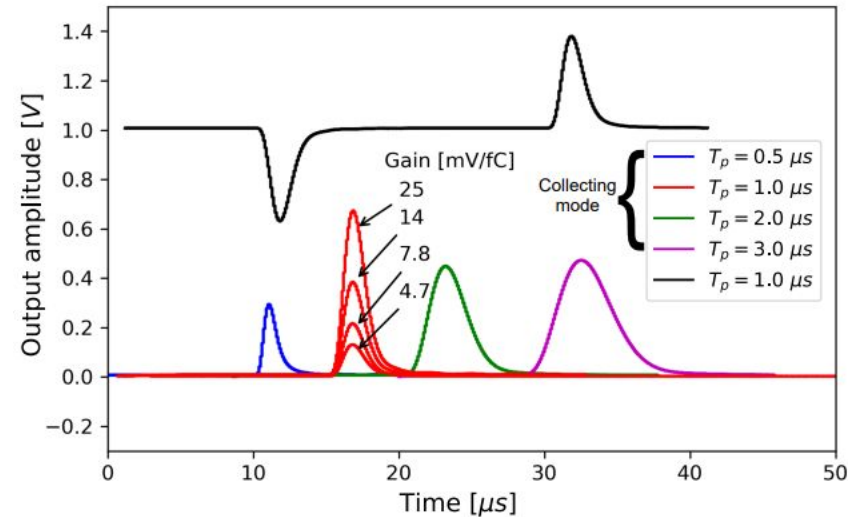
8" wafer with 610
LARASICs P5 and
P5A(B) w. increased
ESD protection

250 wafers LArASIC production run
for DUNE 75k P5 and 75k P5B chips

LArASIC measurement results [1]

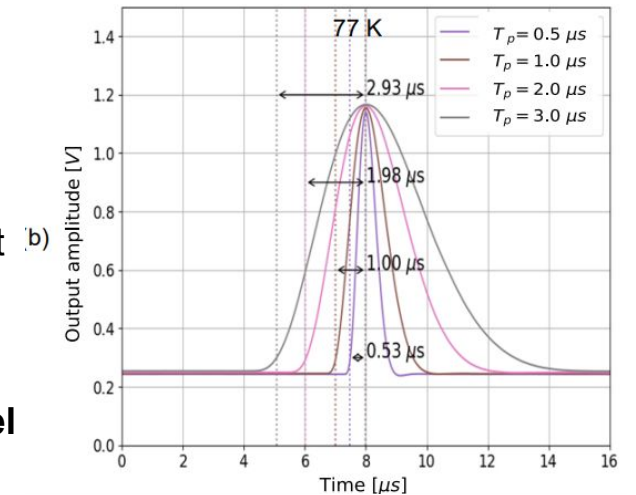
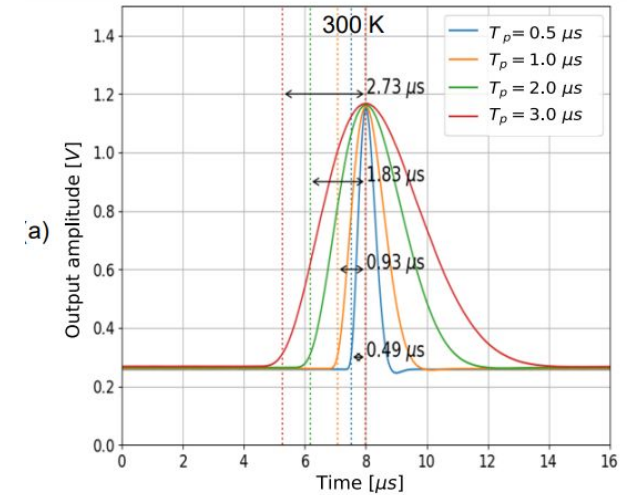


Measurement setup



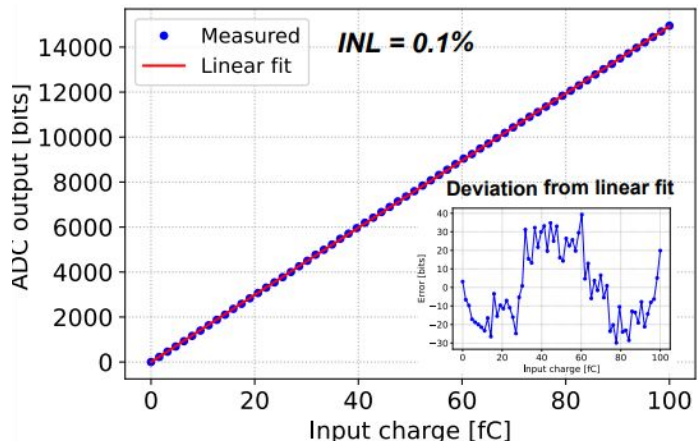
Oscilloscope outputs at 77 K

- Test pulse charge inputs with programmable amplitudes provided either by on-chip 6-bit DAC or external source
- On-chip MiM capacitor calibrated to be 186 fF with less than 1% channel-to-channel dispersion at RT and LNT included in test input path
- Application of variable-amplitude voltage pulse injects known charge into the channel
- Full-scale range of DAC programmable based on gain setting
- **Very small deviations seen between RT and LNT in the measured peaking time and channel gain (< 2%)**

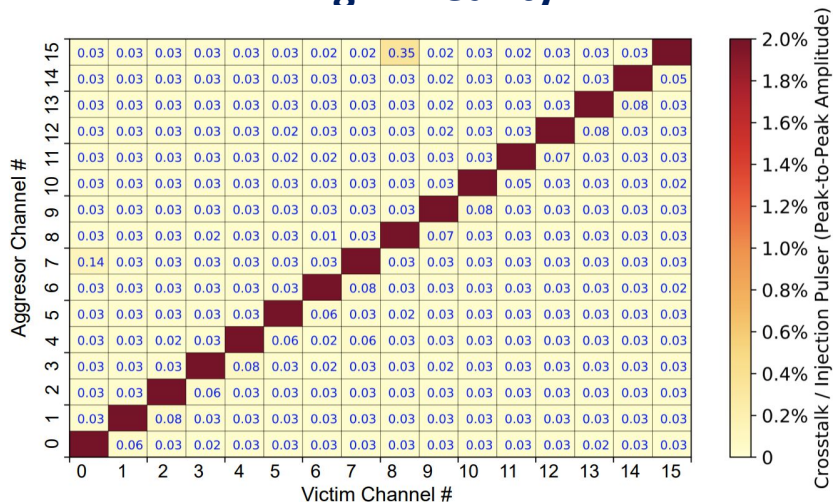


Measured peaking times

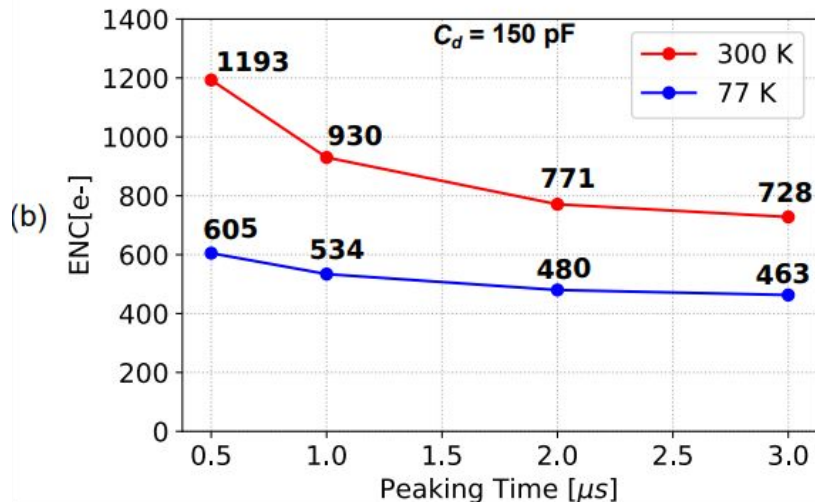
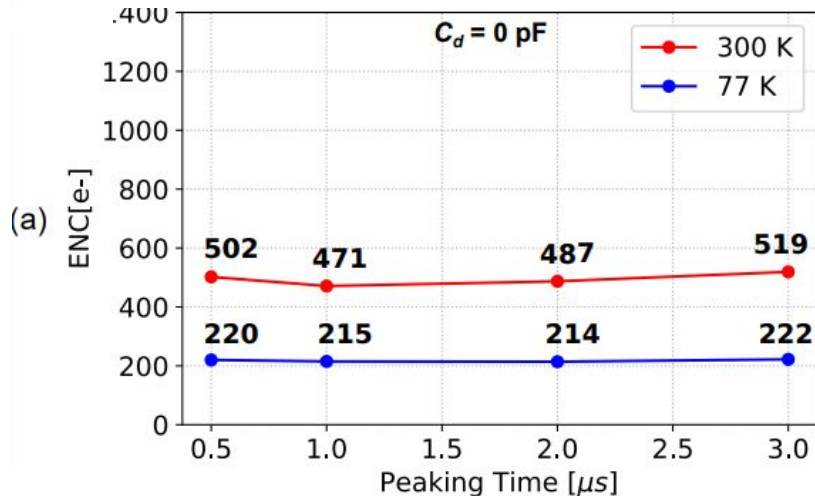
LArASIC measurement results [2]



High linearity



Low inter-channel
crosstalk (mean: 0.04%)



Low noise

TABLE III: Measured power consumption

Temperature	Baseline	Power consumption (mW)		
		Buffers off	SE on	SEDC on
300 K	200 mV	5.6	9.0	10.7
77 K	200 mV	5.3	8.8	10.8
300 K	900 mV	5.8	9.5	10.6
77 K	900 mV	5.5	9.1	10.5

Power consumption

Specifications for CHARMS250

Technology	65 nm CMOS: 1-poly, 9-metal
Supply voltage	1.8 V
Temperature range	77 K – 300 K (optimized for 89 K)
Number of channels	16
Maximum single-ended output swing	1.4 V peak to peak
Gain	4.7 mV/fC, 7.8 mV/fC, 14 mV/fC, 25 mV/fC
Full-scale input charge	300 fC, 180 fC, 100 fC, 56 fC
Baseline selection	200 mV (unipolar, collection mode), 900 mV (bipolar, induction mode)
Adaptive reset current	0.1 nA, 0.5 nA, 1 nA, 2 nA
Peaking time	250 ns, 500 ns, 1 μ s, 2 μ s
Output coupling	DC, AC
Output drive	Shaper, single-ended buffer, differential buffer
Integrated test capacitor	200 fF
Integrated pulse generator	10-bit DAC based
Configuration control	I ² C based for providing digital assistance (programmable gain, peaking time, baseline, and Reset Quiescent Current or RQI)

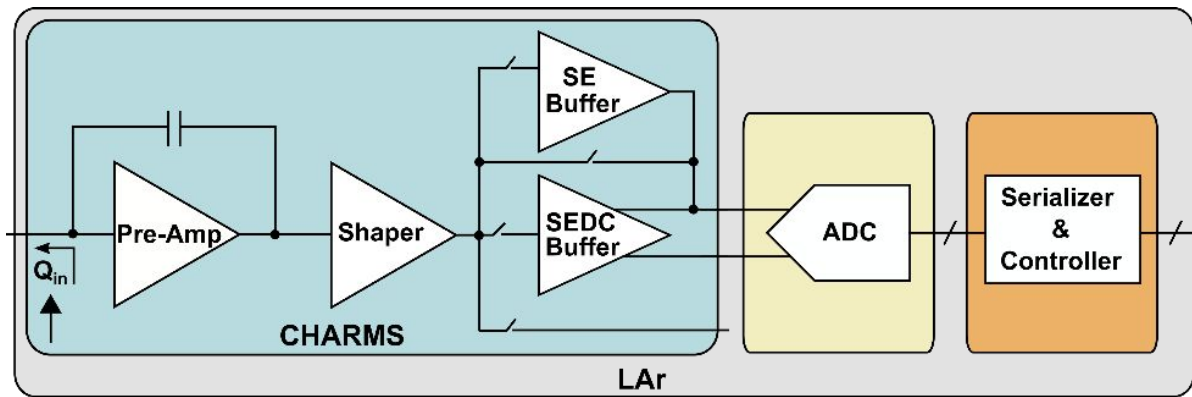
CHARMS10 (peaking time range 10-200 ns) also planned for development

- **Key features and challenges**

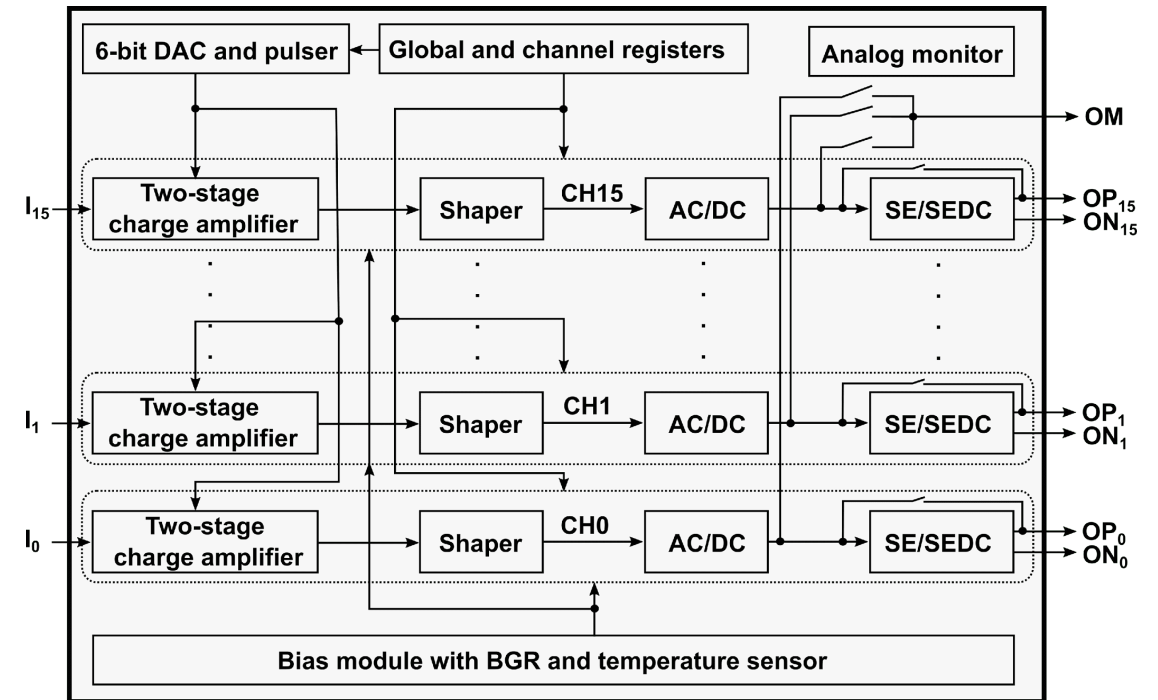
- **65 nm** CMOS with **thick oxide** → To limit gate leakage current and **parallel noise contribution**
- **Low** power consumption (6-11 mW per channel) → support detector electrodes with **fine segmentation**
- **Cryogenic** operation with **long lifetime of electronics** → achieve optimum **SNR**

Architecture and functionality

3-ASIC solution

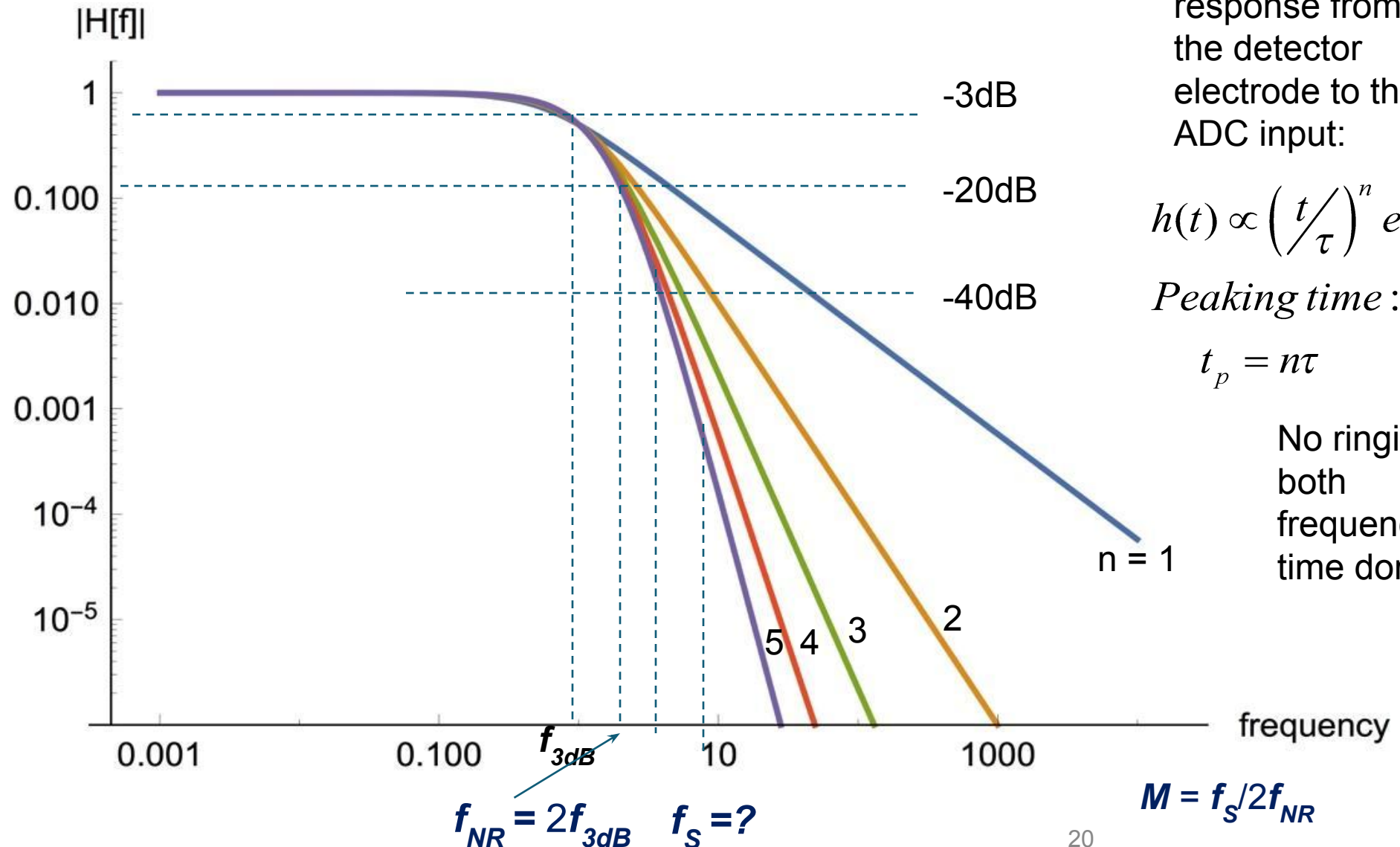


CHARMS Top-level block diagram

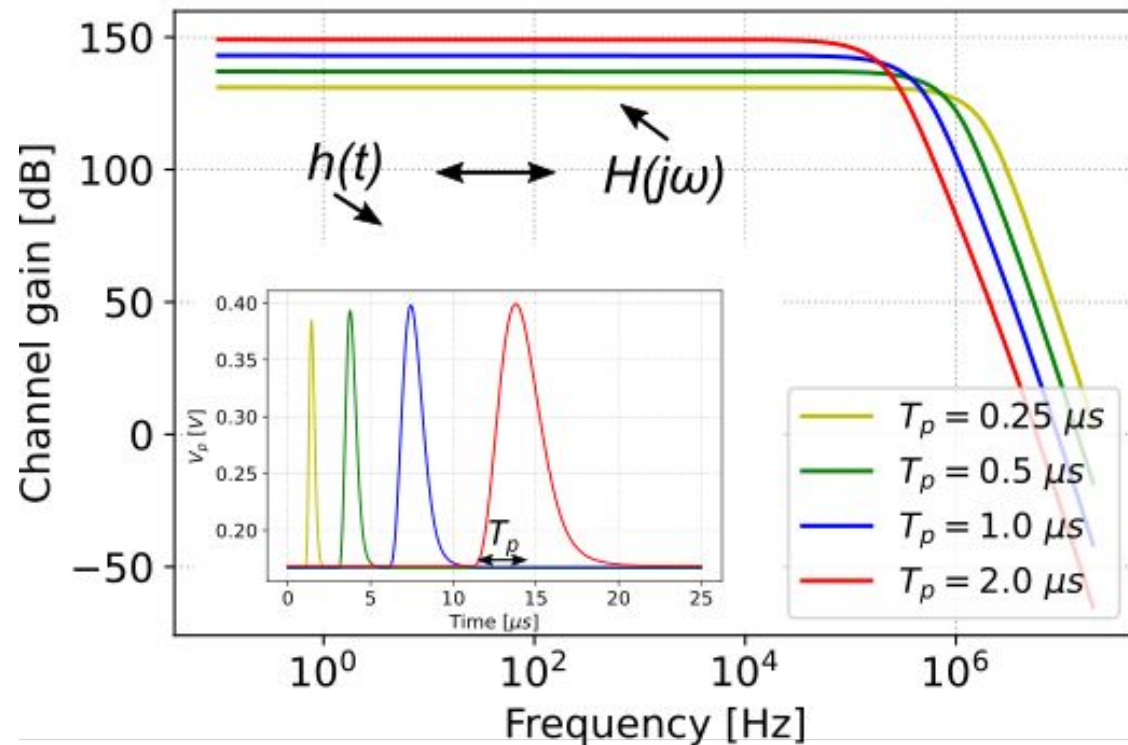


Front-end ASIC (CHARMS) acts as an anti-aliasing filter

Poisson (“semi-Gaussian”) low-pass filters of increasing order: $n = 1, \dots, 5$



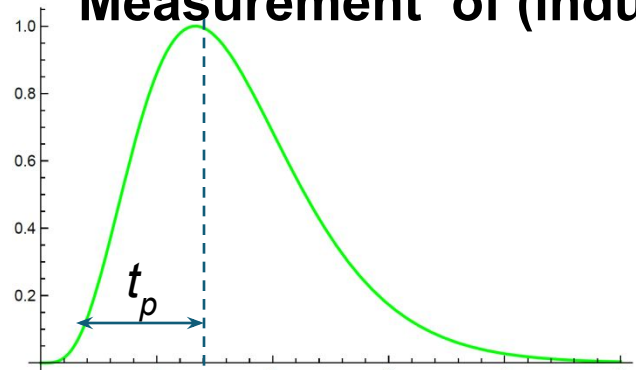
CHARMS250 overall channel impulse response



Peaking time (T_p)	Cut-off frequency (f_{3dB})	Sampling frequency ($f_s = 2/T_p$)	Gain change at f_s	
0.25 μs	820 KHz	8 MHz	-79 dB	2.4
0.5 μs	411 KHz	4 MHz	-71 dB	2.4
1.0 μs	205 KHz	2 MHz	-68 dB	2.4
2.0 μs	102 KHz	1 MHz	-66 dB	2.4

Shaping filter provides a 5th order response using complex pole pairs

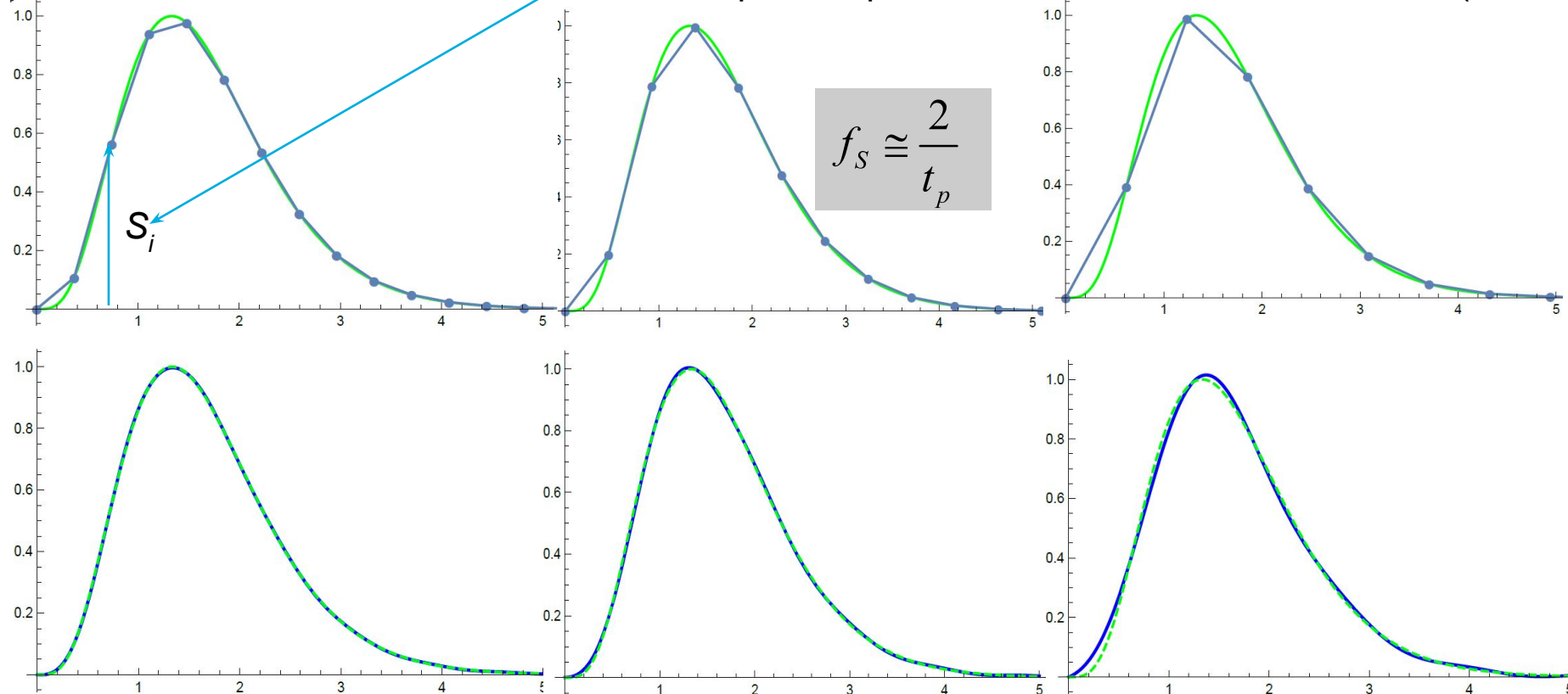
Sampling, Waveform Reconstruction and Charge (area) Measurement of (induced) current $i(t)=q\delta(t)$, from the samples



$$M = f_S / 2f_{NR} = f_S / 4f_{3dB} = \text{sampling frequency} / (4 \times 3\text{dB bandwidth})$$

$$\Delta q / q = \left[\sum S_i - \int h(t) dt \right] / \int h(t) dt = \text{charge (area) error}$$

Waveform interpolating function = **$\sin(x)/x$** used on the sampled sequence to reconstruct the waveforms (bottom row):

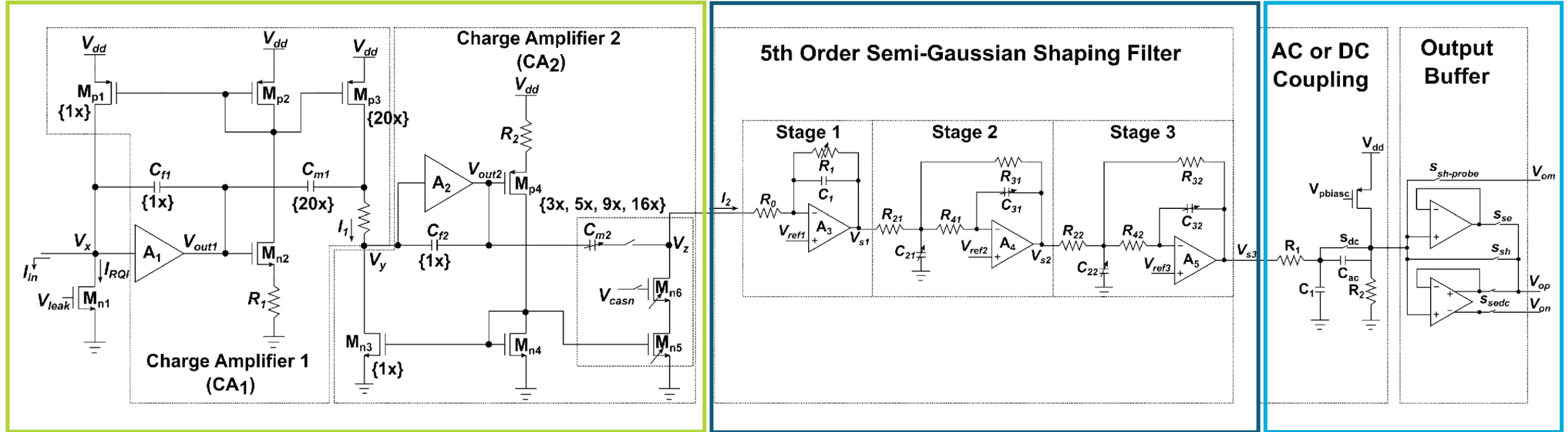


$$M = 2.5 \quad \Delta q / q = 0.0011\%$$

$$M = 2 \quad \Delta q / q = 0.0850\%$$

$$M = 1.5 \quad \Delta q / q = 0.3683\%$$

CHARMS250 core channel circuits



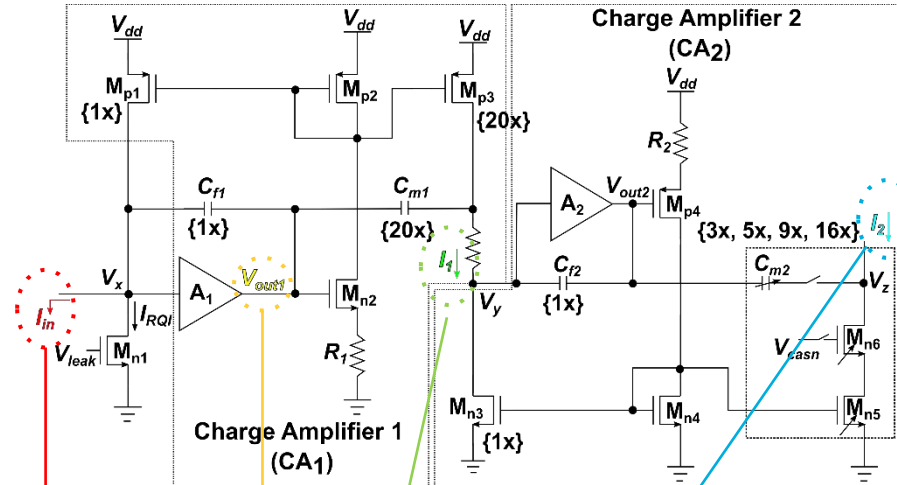
Amplification

Filtering

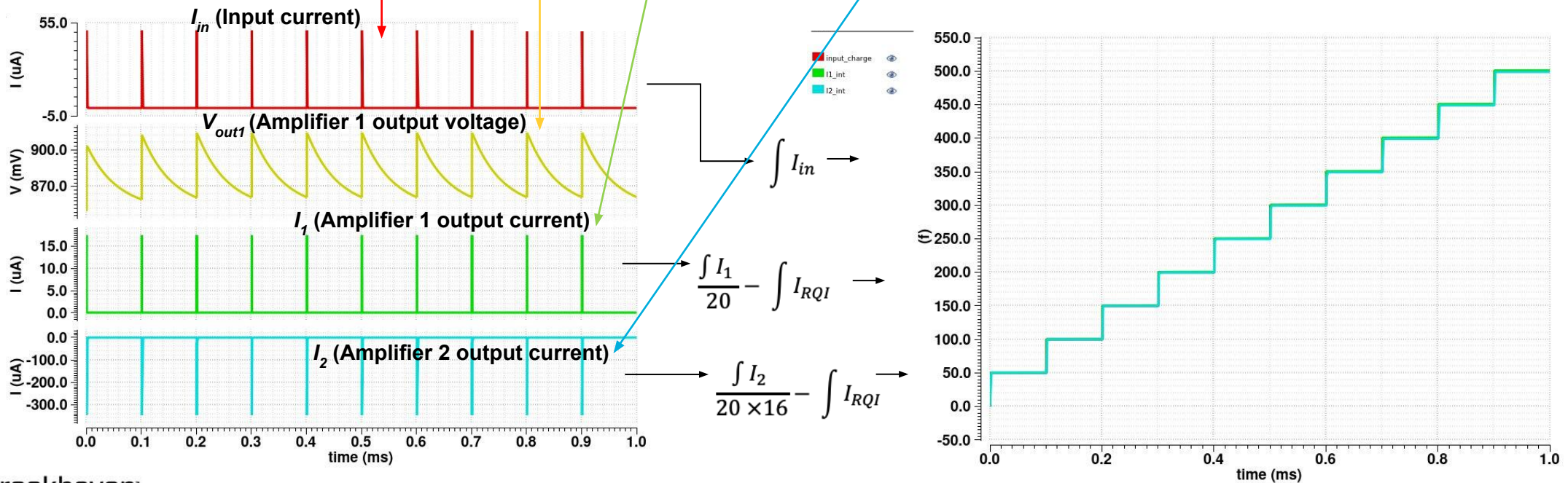
Output drive

Charge amplifier design and transient response

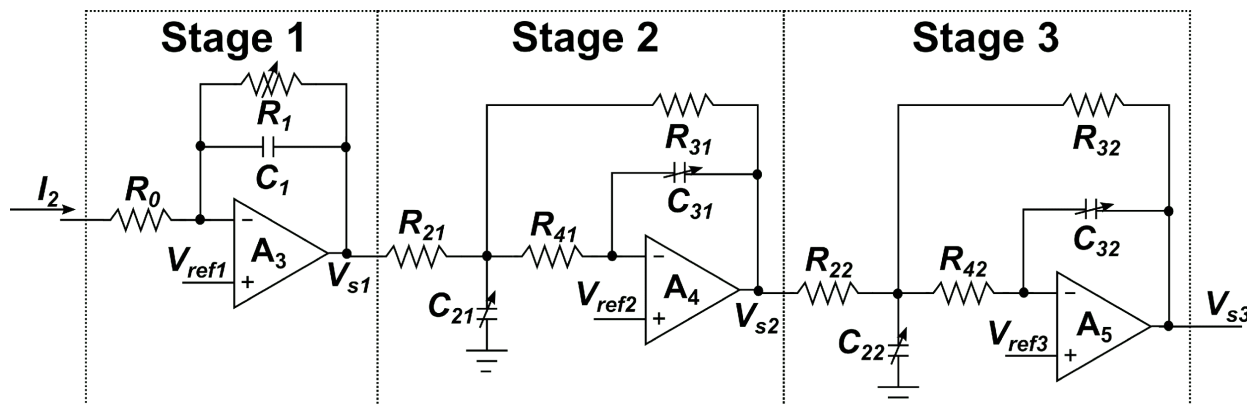
- Charge amplifiers use current-mirror based adaptive continuous reset ($I_{RQI} = 100 \text{ pA}$, 500 pA , 1 nA or 2 nA)
- Pole-zero cancellation implemented in each stage



- A_1 and A_2 : 3-stage amplifiers ($> 100 \text{ dB}$ gain for each, at both room and LAr temperatures)
- Charge gain provided by $CSA_1 = 20$
- Charge gain (programmable) provided by $CSA_2 = 3$ or 5 or 9 or 16

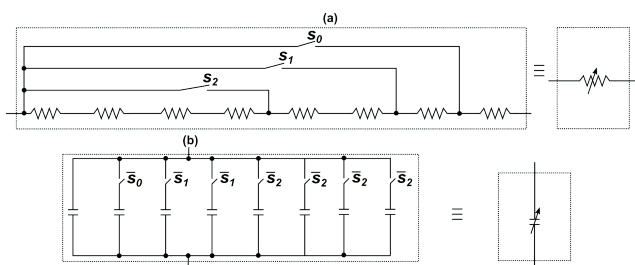


Shaping filter design



Component values for CHARMS250

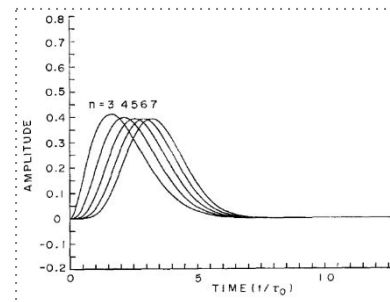
Resistor	Value (kΩ)	Capacitor	Value (pF)
R_0	0.3		
$R_u (R_1)$	7.5	C_1	11.9
R_{21}, R_{41}, R_{42}	18	$C_u (C_{21})$	5.9
R_{31}	60	$C_u (C_{31})$	1.39
R_{22}	36	$C_u (C_{22})$	5.5
R_{32}	39	$C_u (C_{32})$	1.13



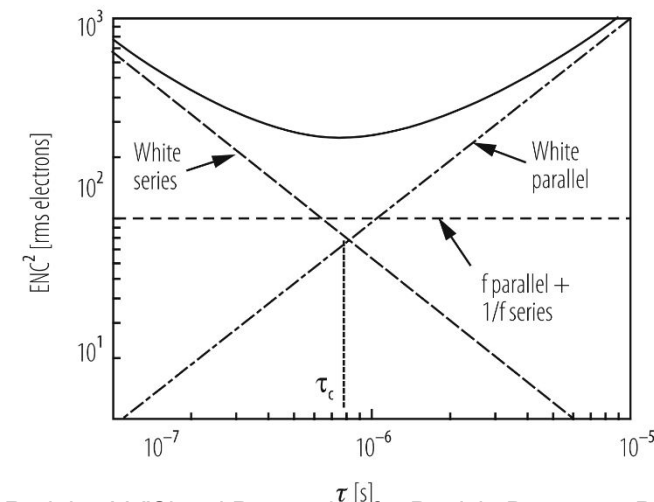
$$V_{s1}(s) = -I_2(s) \frac{R_1}{(1 + sC_1R_1)}$$

$$V_{s2}(s) = -V_{s1}(s) \frac{1}{s^2 + s \left(\frac{1}{R_{21}C_{21}} + \frac{1}{R_{31}C_{31}} + \frac{1}{R_{41}C_{21}} \right) + \frac{1}{R_{31}R_{41}C_{21}C_{31}}}$$

$V_{s3}(s)$ is similar.....



- Peaking time programmable (0.25 μ s – 2 μ s)
- Lower series noise with longer shaping times
- Implemented shaper is a 5th order semi-Gaussian filter with complex conjugate poles
 - Faster return to baseline than CR-RCⁿ filters
 - Faster tail lowers contribution of parallel noise
 - Symmetric rising and falling edges also helpful for mitigating pile-up of events
- A_3, A_4, A_5 are two-stage Miller-compensated differential amplifiers
- $V_{ref1}, V_{ref2}, V_{ref3}$ selected based on output

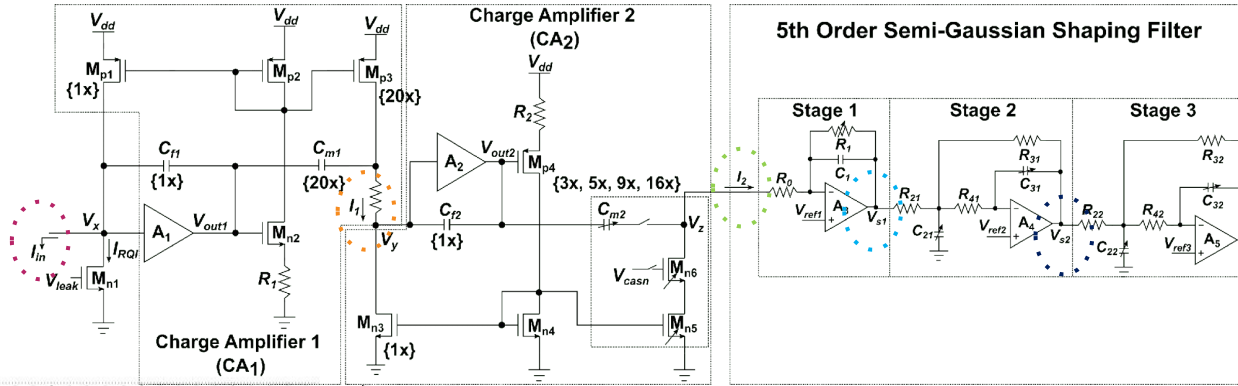


Radeka, V. "Signal Processing for Particle Detectors: Particle Detectors and Detector Systems." *Detectors for Particles and Radiation. Part 1: Principles and Methods* (2011): 288-319.

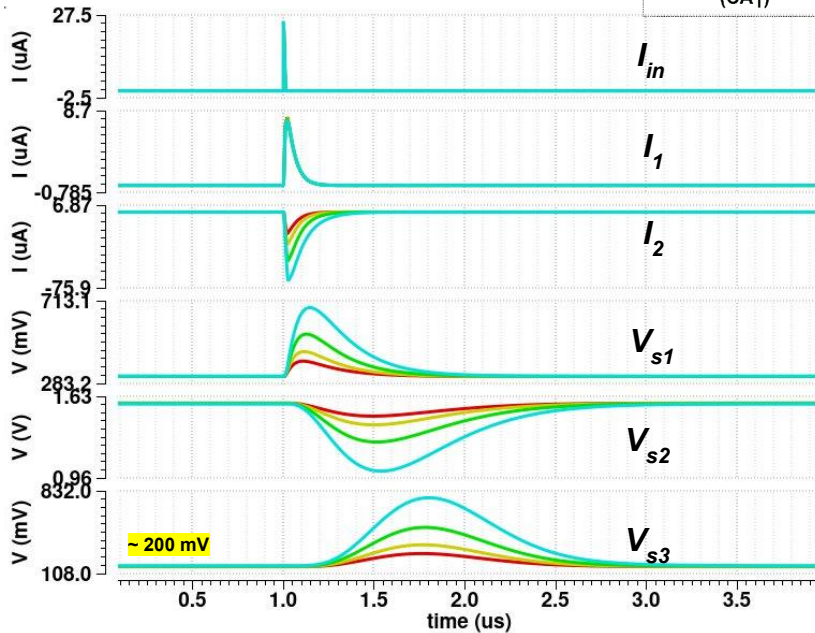
Ohkawa, S., M. Yoshizawa, and K. Husimi. "Direct synthesis of the Gaussian filter for nuclear pulse amplifiers." *Nuclear Instruments and Methods* 138.1 (1976): 85-92.

Simulated impulse response of analog chain at LArT

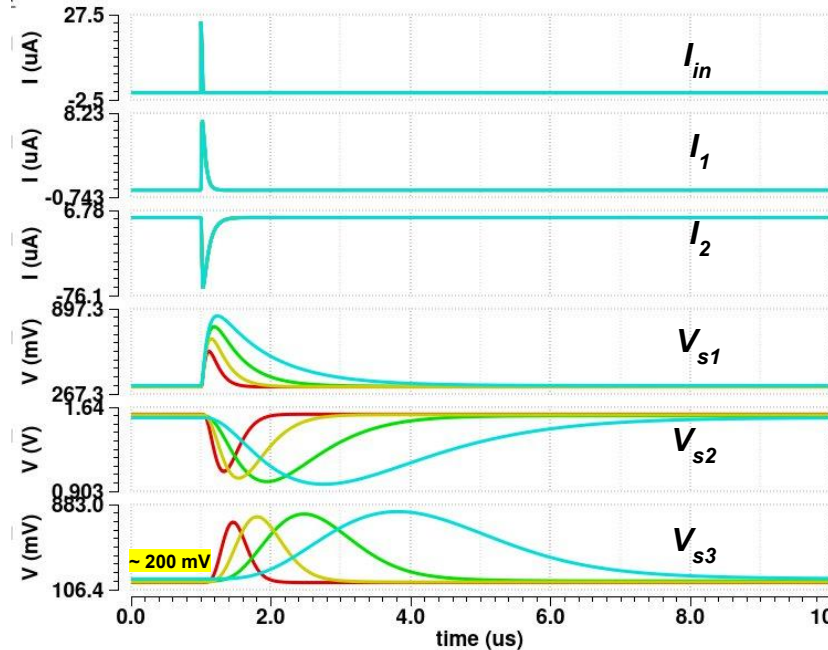
I_{in} : Input current
 I_1 : Amplifier 1 output current
 I_2 : Amplifier 2 output current



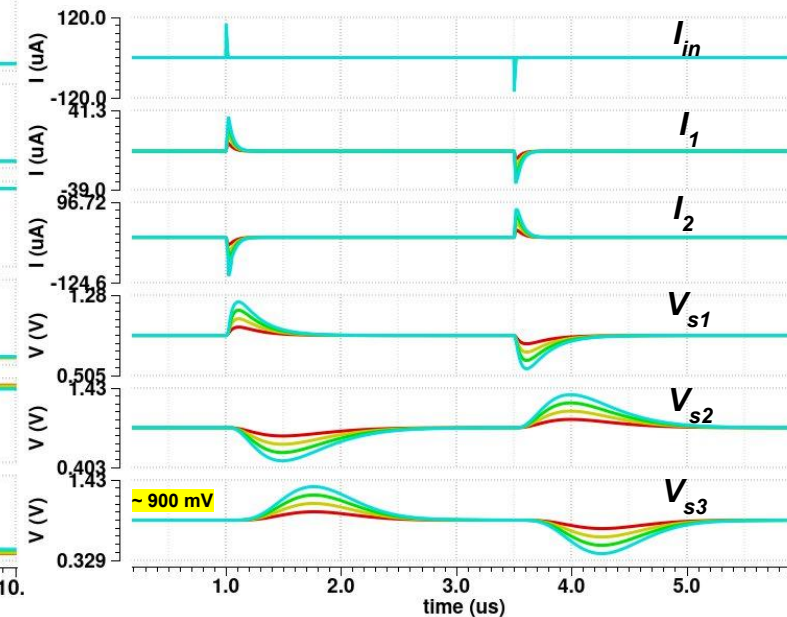
V_{s1} : Shaper stage 1 output voltage
 V_{s2} : Shaper stage 2 output voltage
 V_{s3} : Shaper stage 3 output voltage



Programmable gain
 (4.7 mV/fC, 7.8 mV/fC,
 14 mV/fC, 25 mV/fC)



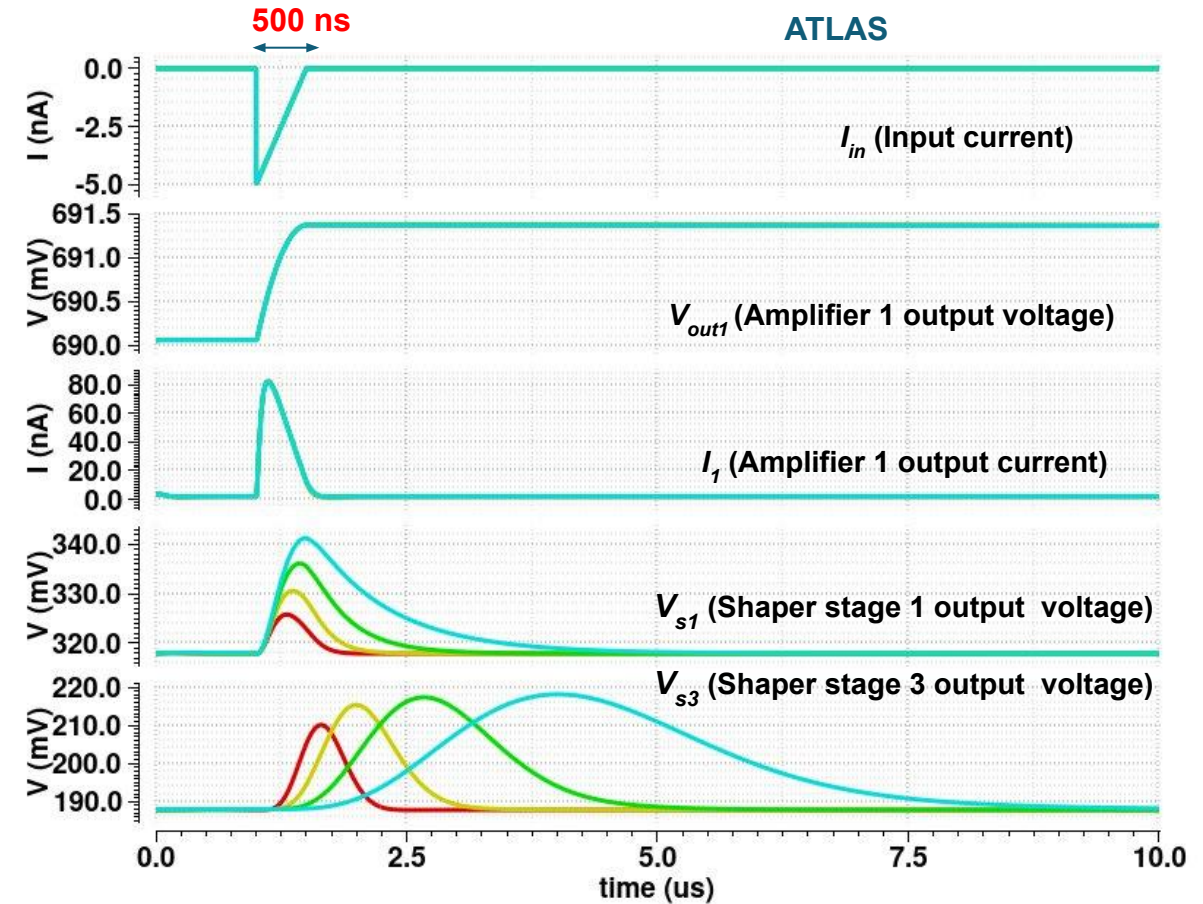
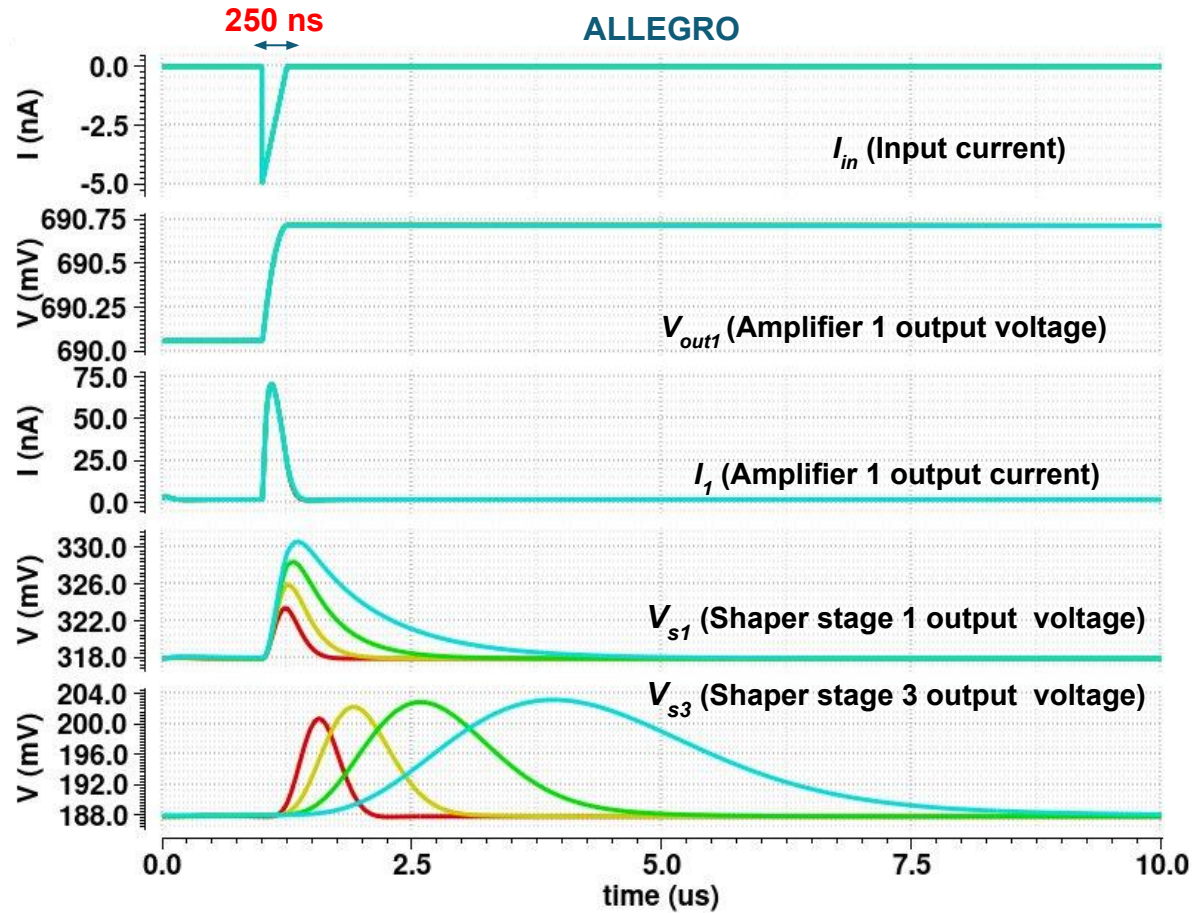
Programmable peaking
 time (0.25 μ s, 0.5 μ s,
 1.0 μ s, 2.0 μ s)



Non-collecting mode
 (Bipolar charges with
 magnitude 25 fC, 50 fC,
 75 fC, 100 fC)

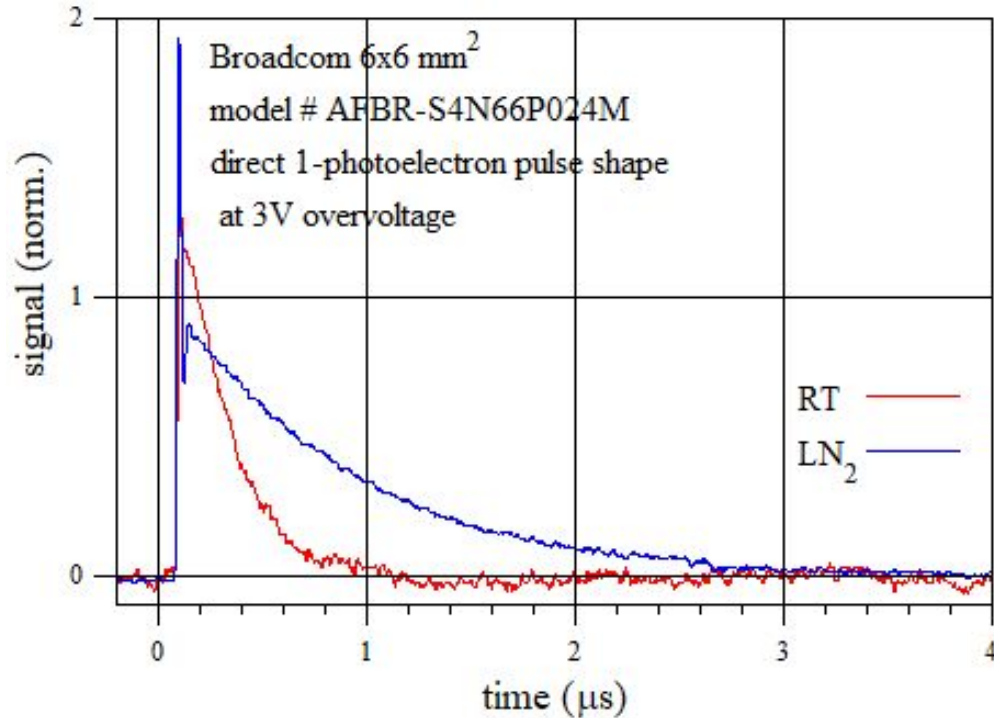
Front-end response to LAr calorimeter triangular current signals

Channel gain = 25 mV/fC, Response for different peaking times (250 ns, 500 ns, 1 μ s, 2 μ s)



Front-end response to SiPM signals

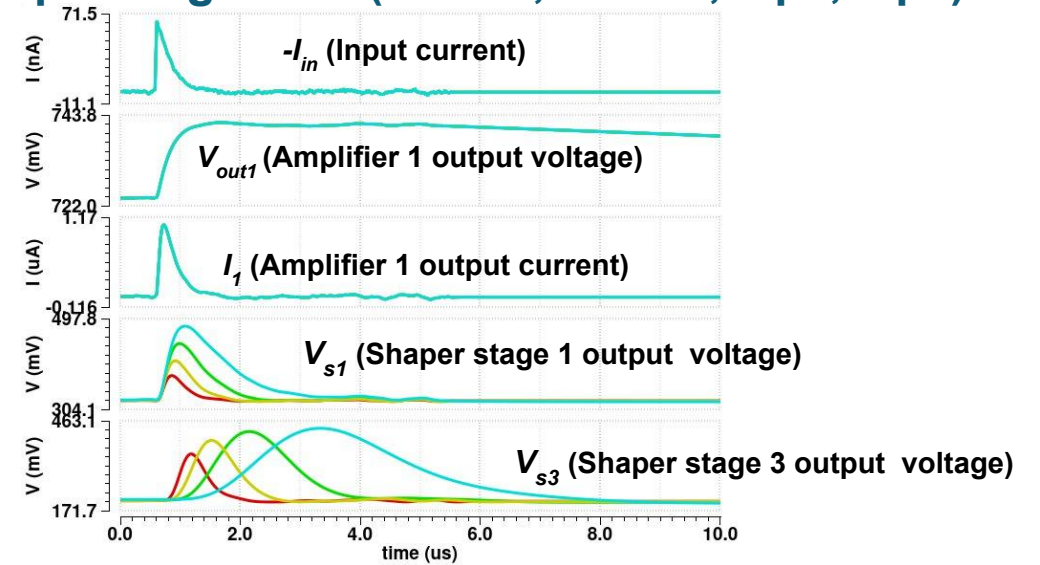
Channel gain = 4.7 mV/fC, Response for different peaking times (250 ns, 500 ns, 1 μ s, 2 μ s)



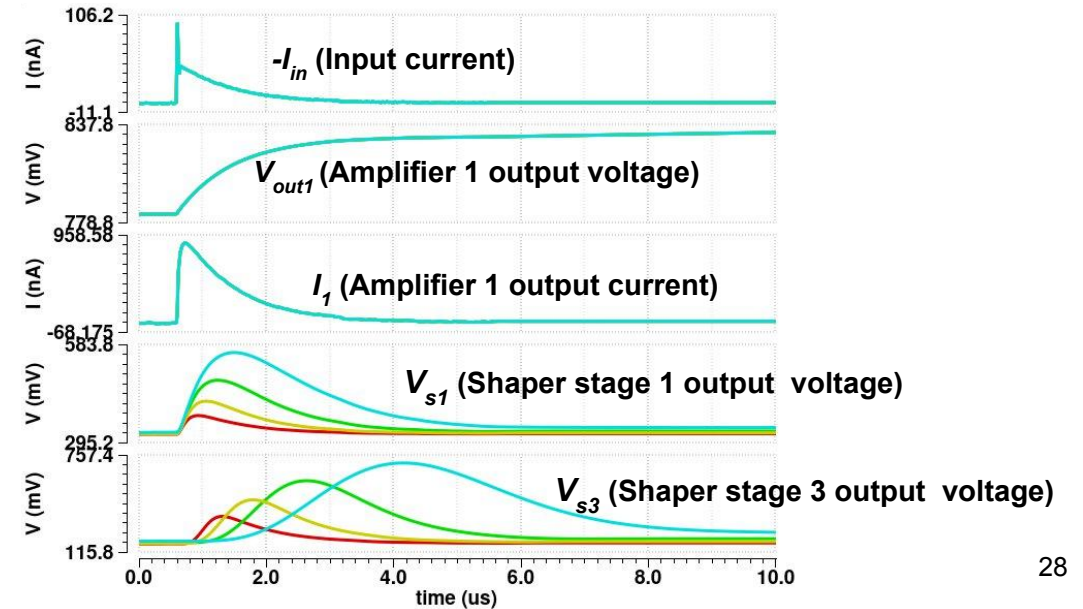
Acknowledgement: T. Tsang

*In these simulations, negative current (electrons) are injected

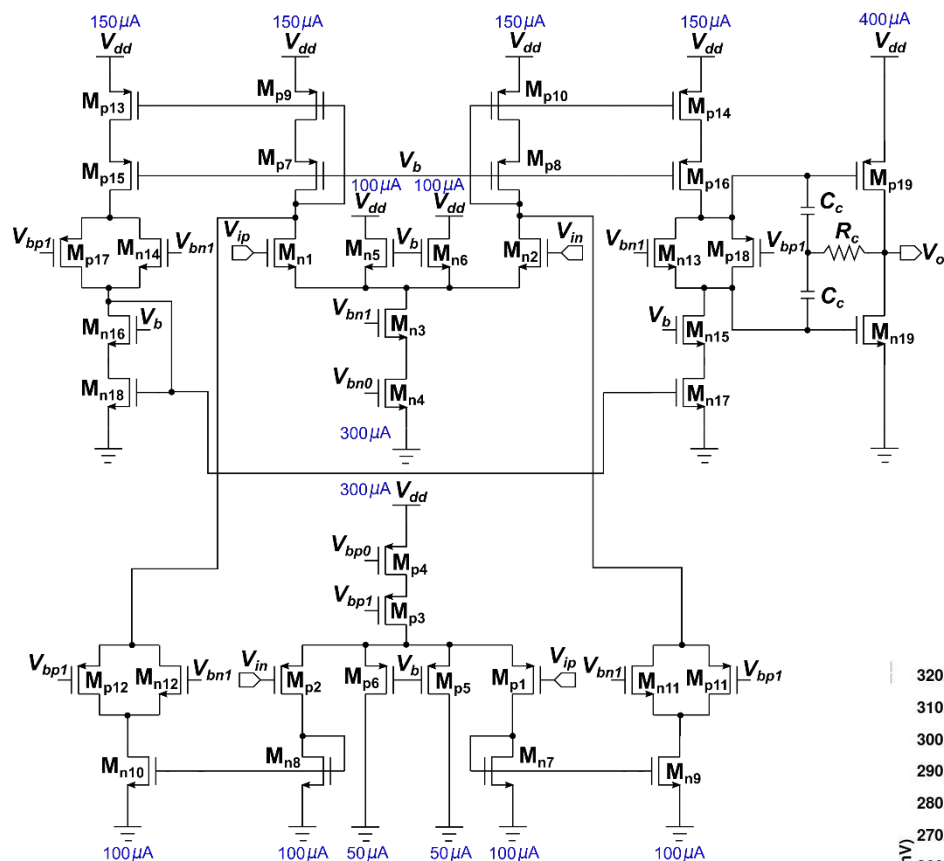
Room temperature



Liquid argon temperature

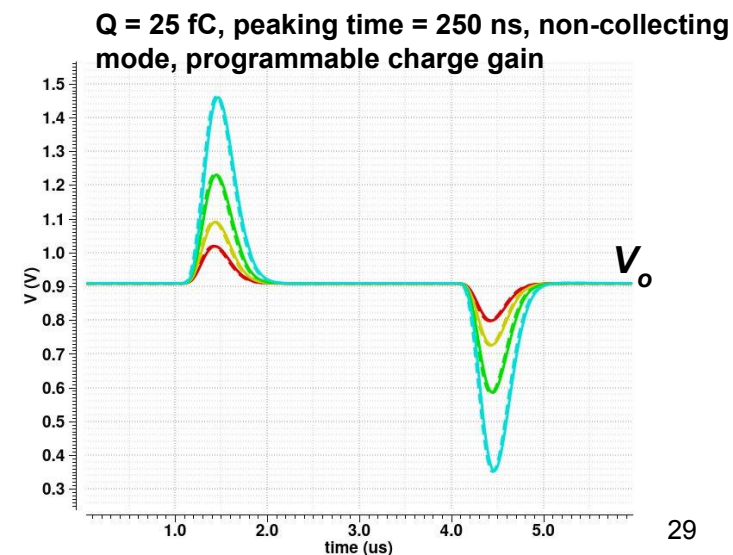
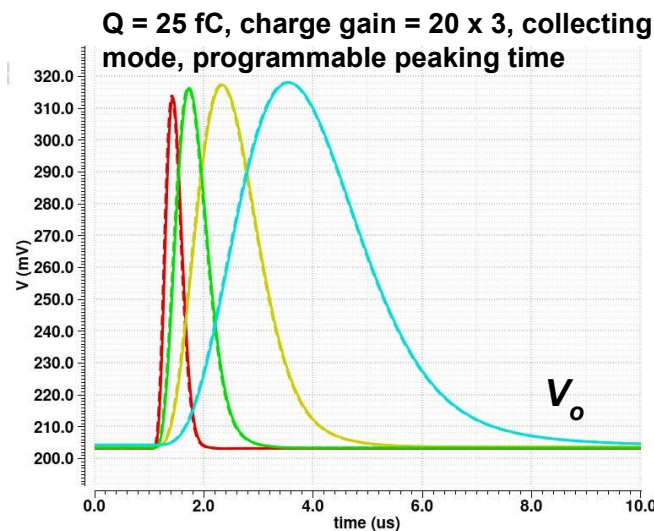


Output buffer design – single ended (SE) buffer



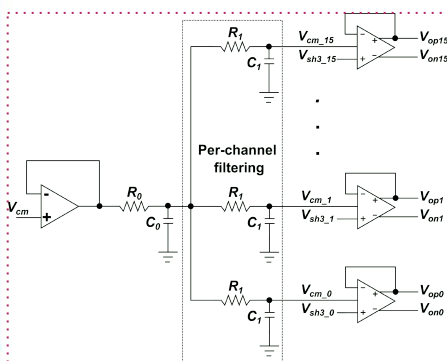
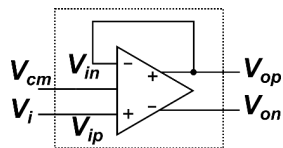
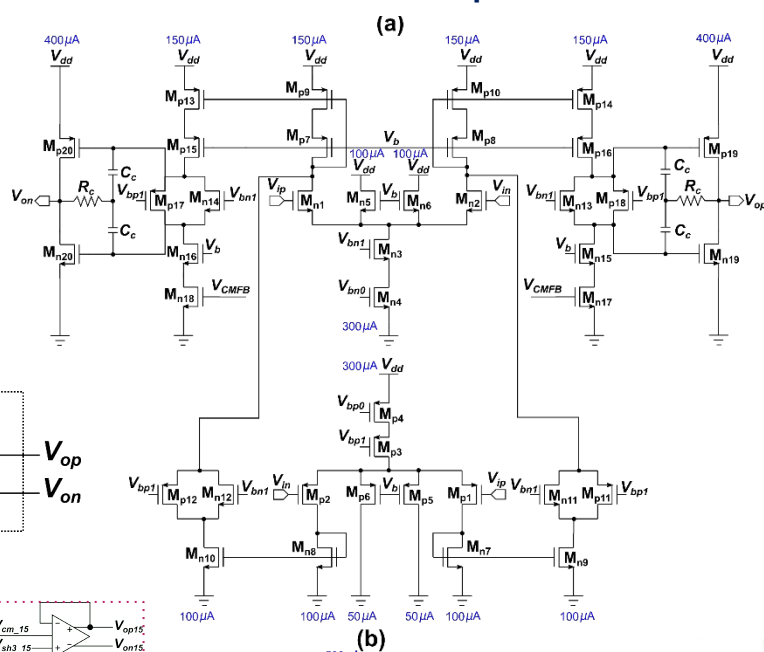
- Based on a folded-cascode current-mirror based operational transconductance amplifier
- Comprises of parallel NMOS and PMOS input pairs to support rail-to-rail operation
- Monticelli class-AB output stage used
- High open-loop DC gain (> 110 dB at LArT) ensures minimal introduction of distortion in the output signal
- Capable of driving tens of pF of capacitive load (typically, chip-to-chip traces)

SE Buffer impulse response with 100 pF load



Output buffer design – differential (SEDC) buffer

Main loop

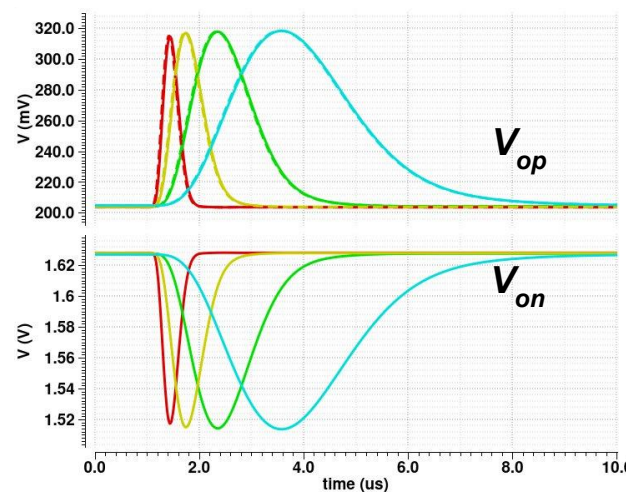


CMFB loop

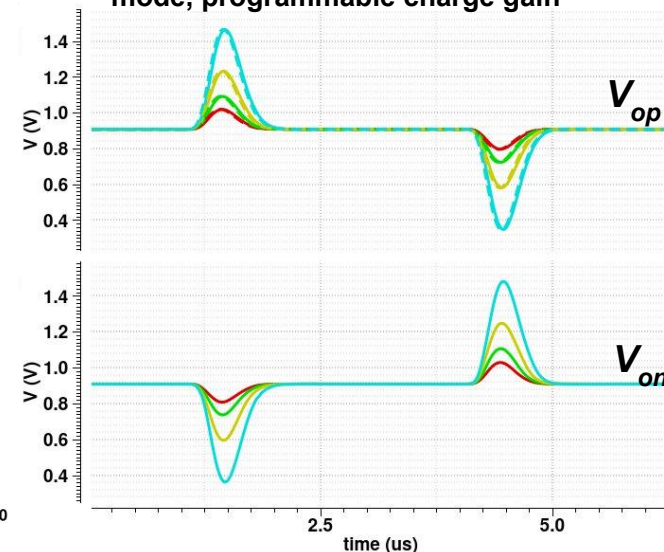
- Simpler, more compact and power-efficient compared to resistor or 3-operational amplifier based single-ended to differential converter (SEDC) designs
- Circuit implementation is similar to SE buffer, but core is fully-differential (inputs and outputs)
- Noise is transferred from the common-mode input signal (V_{cm}) to the output with 6 dB gain
 - Global and local noise filtering implemented for V_{cm}
- Both common-mode and differential paths have high open loop DC voltage gains (> 110 dB) and comparable bandwidths (≈ 100 MHz) at LArT
 - Helps with crosstalk cancellation

SEDC buffer impulse response with 100 pF load

$Q = 25$ fC, charge gain = 20×3 , collecting mode, programmable peaking time

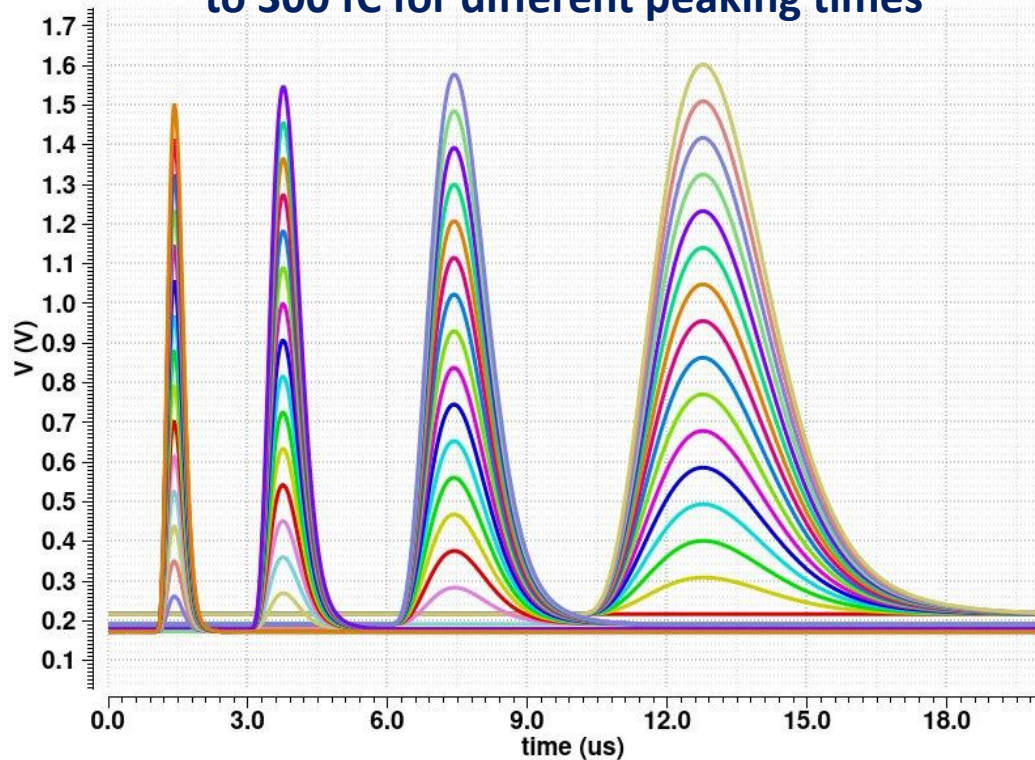


$Q = 25$ fC, peaking time = 250 ns, non-collecting mode, programmable charge gain

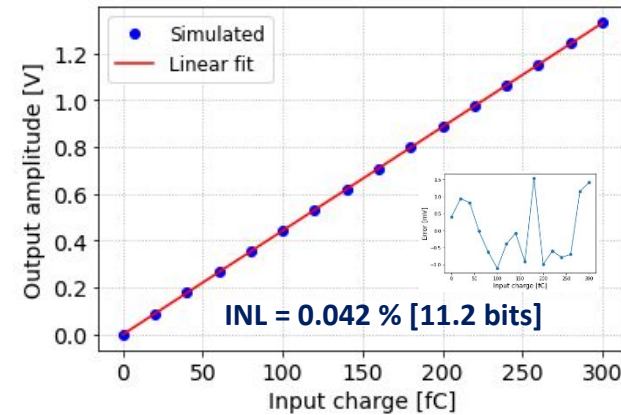


Simulated response for full-charge range and linearity

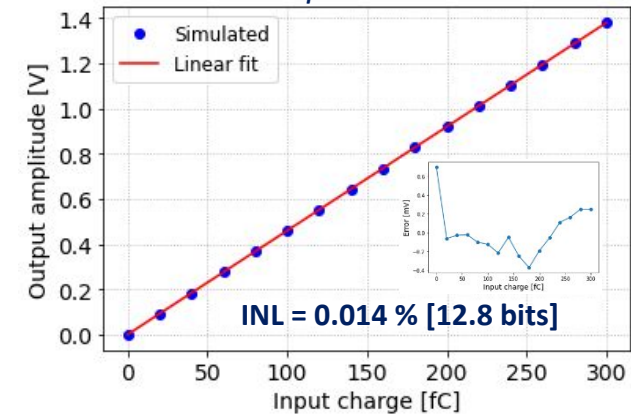
Shaping filter output (V_{s3}) for input charges up to 300 fC for different peaking times



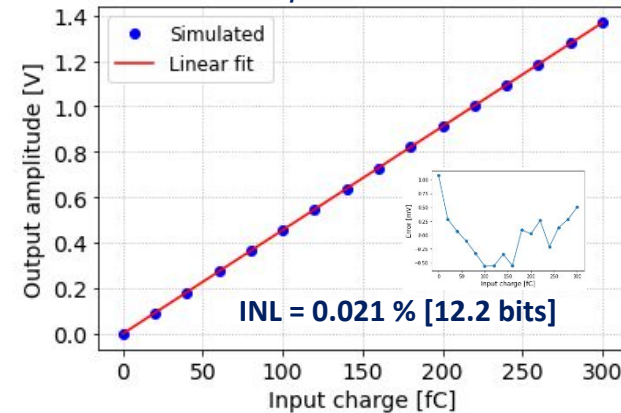
$T_p = 0.25 \mu$ s



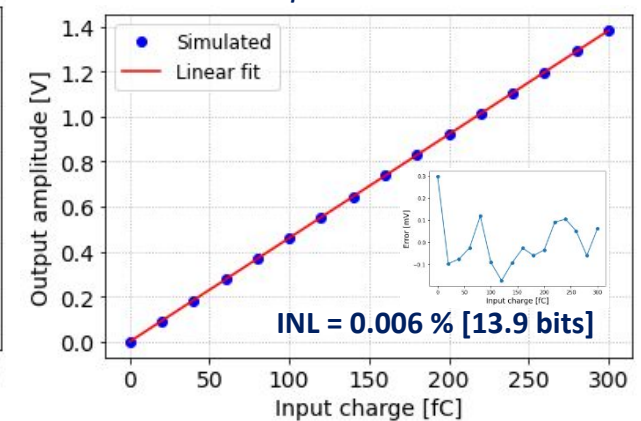
$T_p = 1.0 \mu$ s



$T_p = 0.5 \mu$ s



$T_p = 2.0 \mu$ s



Noise minimization strategy

- Input-referred charge noise = Equivalent Noise Charge (ENC)

$$ENC^2 = (C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_f K_f \right) + A_p i_n^2 T_p$$

(Sum of **white series noise**, **1/f series noise** and **parallel noise** components)

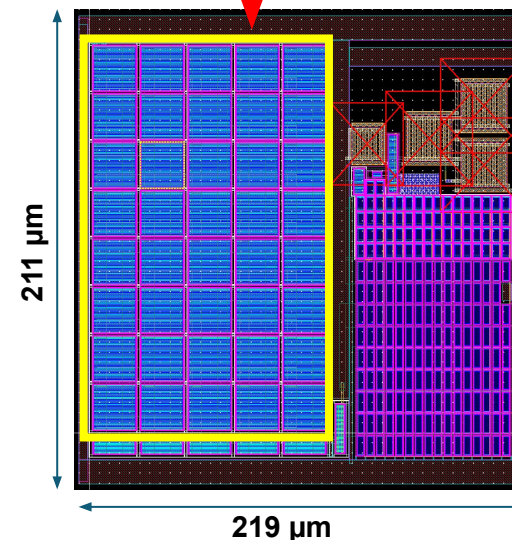
$$ENC_f^2 = K_f \frac{(C_d + C_g)^2}{C_g} N_f \Rightarrow C_g = C_d$$

$$ENC_w^2 = 4k_B T n \gamma \alpha_w \frac{(C_d + C_g)^2}{g_m(C_g)} N_f \Rightarrow C_g = \frac{1}{3} C_d$$

Input transistor implemented with 30 copies of transistors of width of 20 μm and 40 fingers

Input stage transistor sized to have $C_g \sim 40$ pF, optimal choice for minimizing noise with $C_{\text{det}} \sim 150$ pF with given power budget

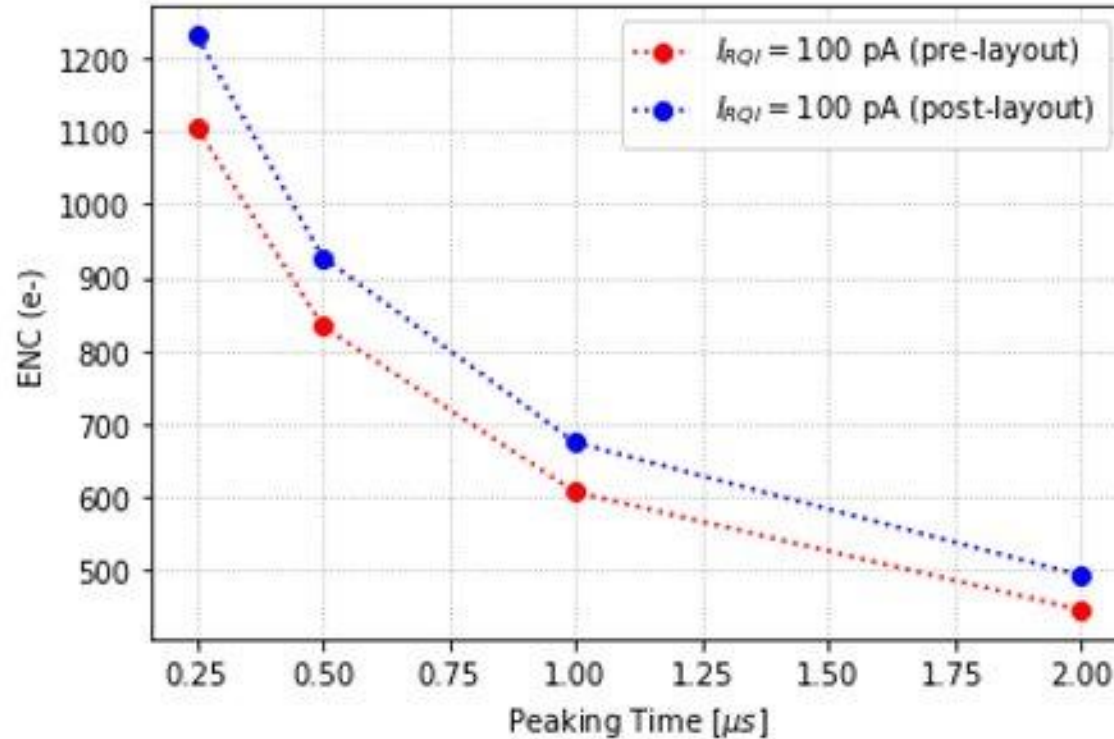
	Minimum allowable transistor length	Input transistor length	Input transistor width
180 nm (LArASIC)	180 nm	270 nm	20 mm
65 nm (CHARMS250)	280 nm	400 nm	24 mm



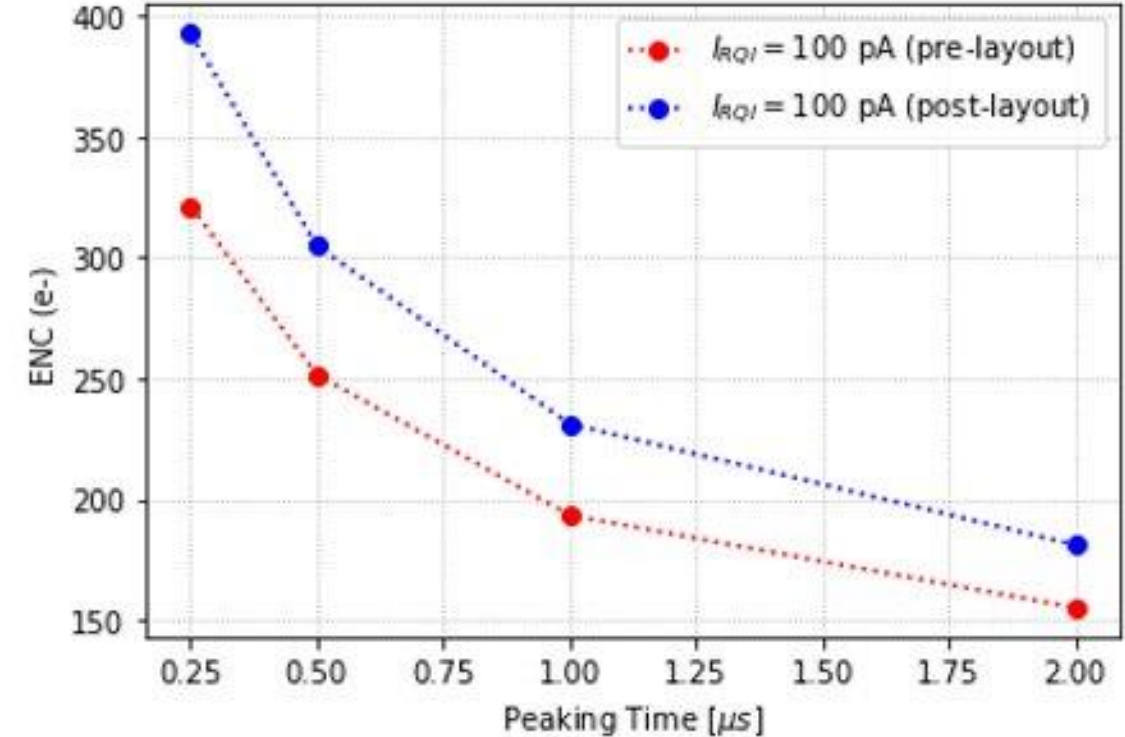
- Input stage transistors for A_1 implemented using thick oxide (2.5 V) devices in 65 nm for CHARMS to limit leakage current and associated **parallel noise**
- Thin oxide device of the same dimensions has a gate leakage current of ≈ 20 nA, contributing almost 200 electrons to the ENC for 1 μs peaking time and triangular weighting function!

Noise (simulated) with $C_d = 160$ pF

Room temperature



Liquid argon temperature



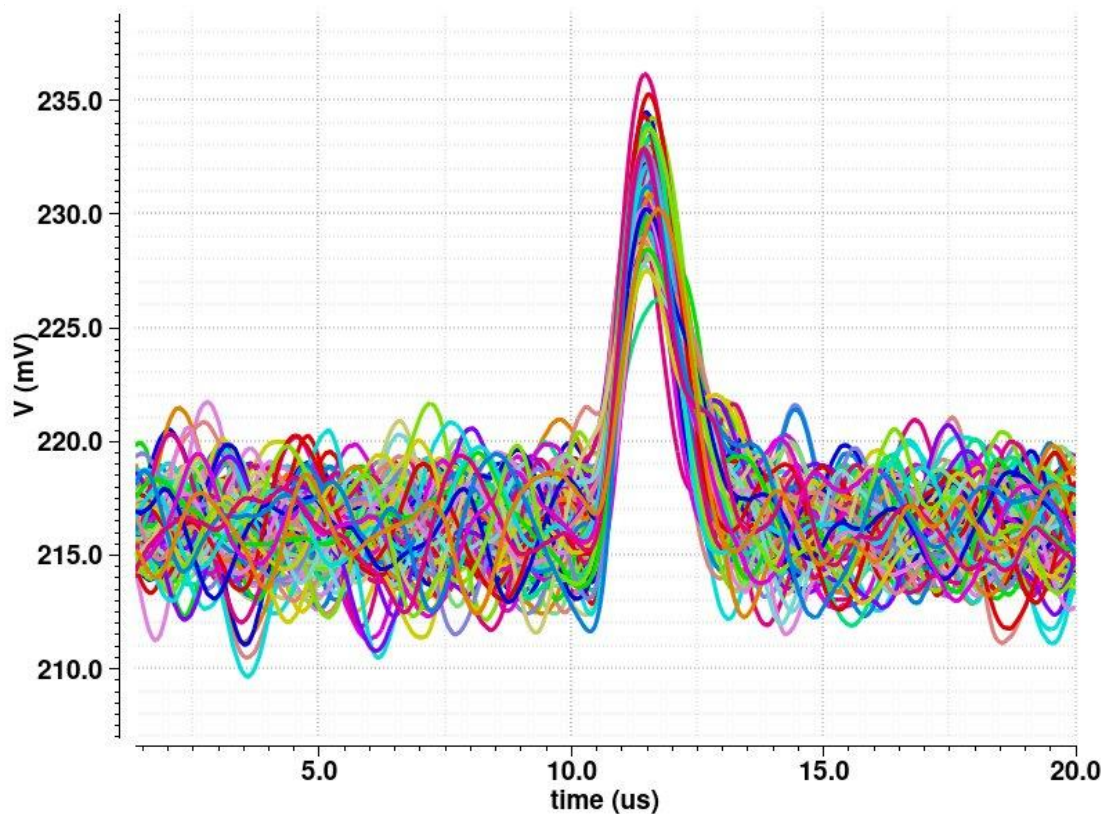
- **Summary:** 60-75% noise contributed by the input transistor (thermal noise contribution dominates, flicker noise contribution is less than 5 %)
- These simulations may be too optimistic since cryogenic $1/f$ noise models of the 65 nm process are unavailable
- Noise characterization needs to be done at liquid argon temperature

(Noisy) Front-end response to LAr calorimeter triangular current signals

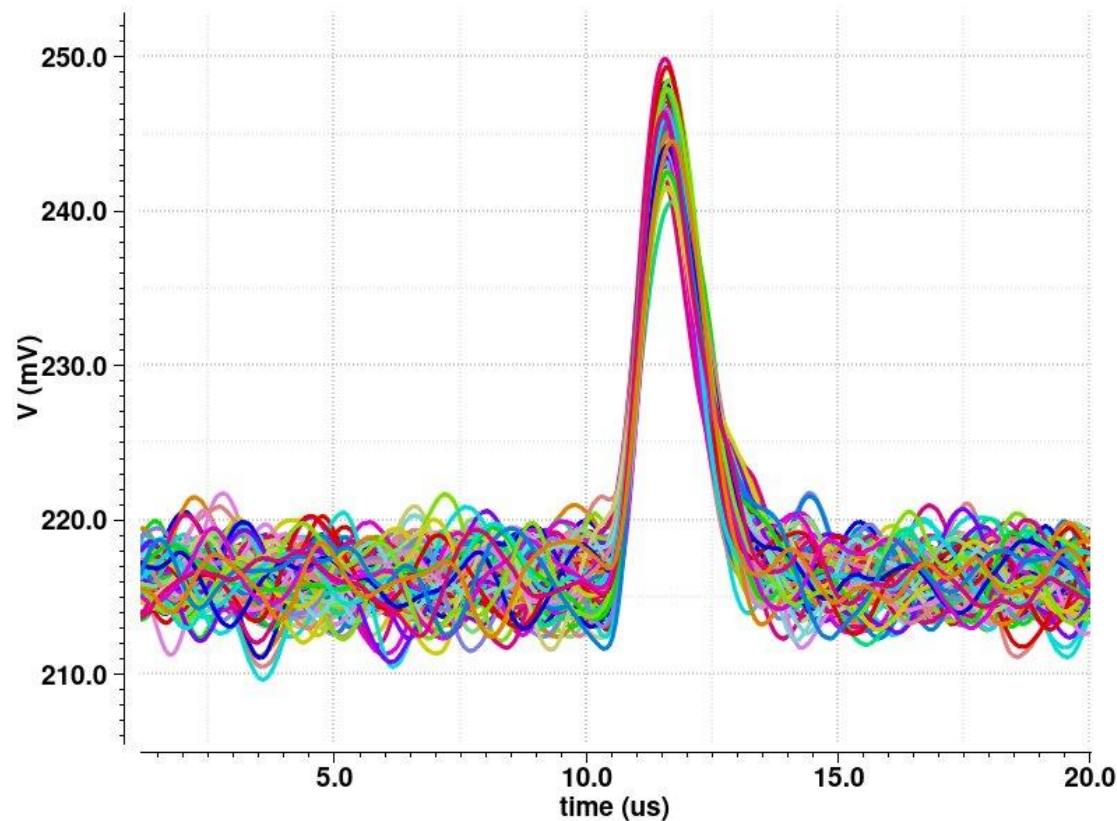
Channel gain = 25 mV/fC, Noisy response for peaking time of 1 μ s, input capacitance of 100 pF

At room temperature:

Input current: triangular with 250 ns decay (ALLEGRO)



Input current: triangular with 500 ns decay (ATLAS)

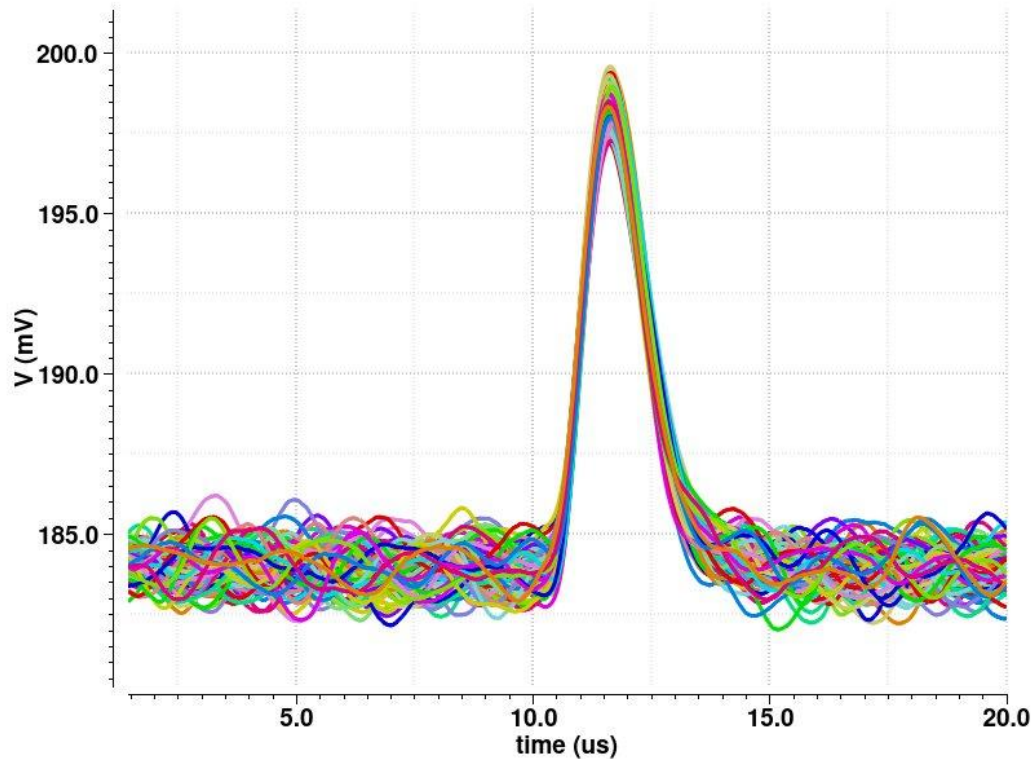


(Noisy) Front-end response to LAr calorimeter triangular current signal

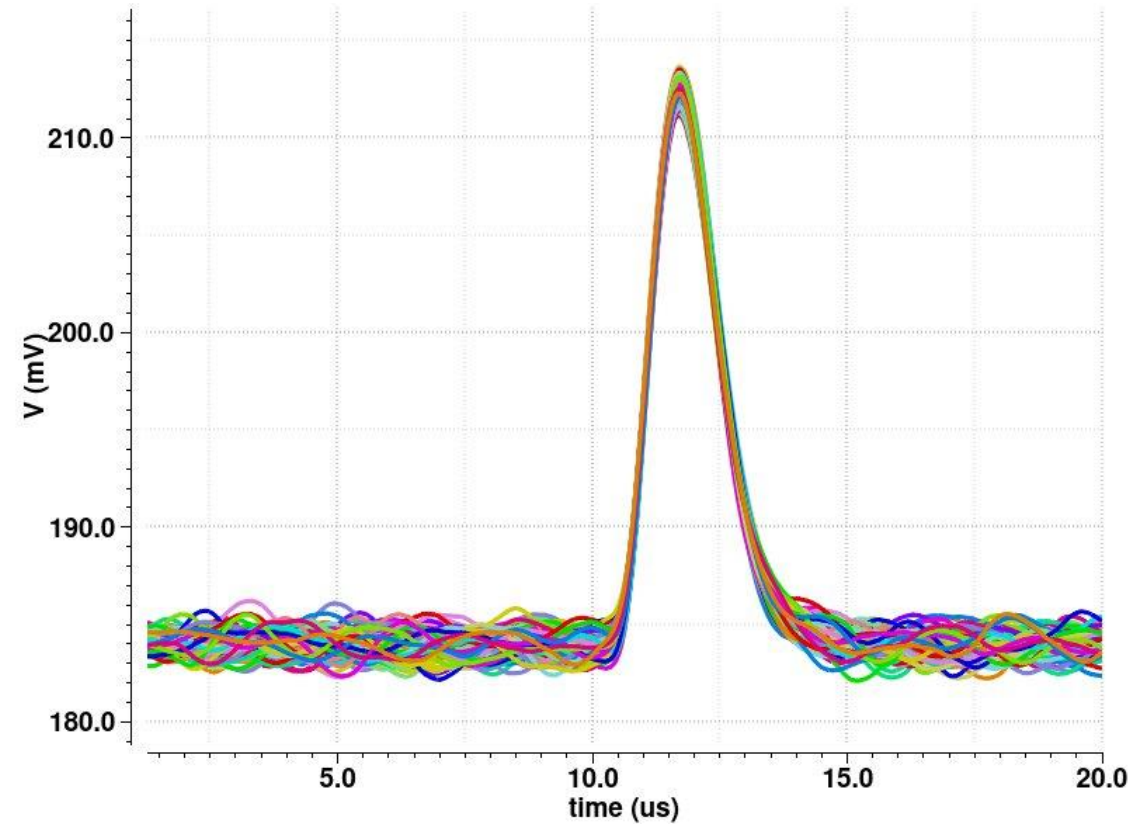
Channel gain = 25 mV/fC, Noisy response for peaking time of 1 μ s, input capacitance of 100 pF

At LAr temperature:

Input current: triangular with 250 ns decay (ALLEGRO)

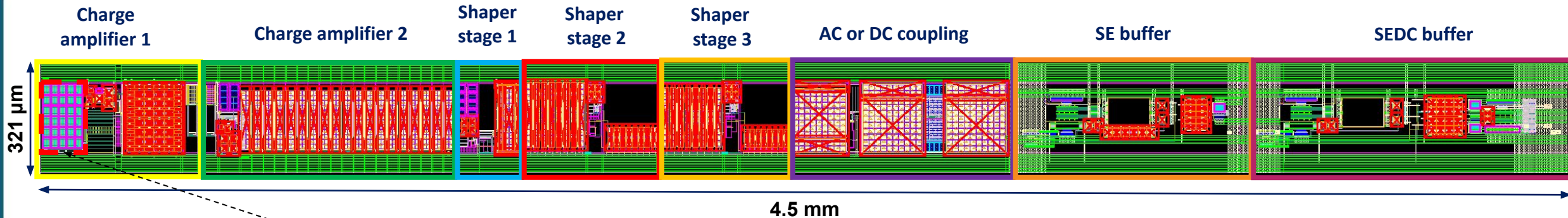


Input current: triangular with 500 ns decay (ATLAS)



CHARMS250 status

Front-end channel layout



Prototype CHARMS250 chip to be submitted for fabrication in June 2025

Transistor test structures with dimensions of the input transistor fabricated for characterization at room and cryogenic temperatures

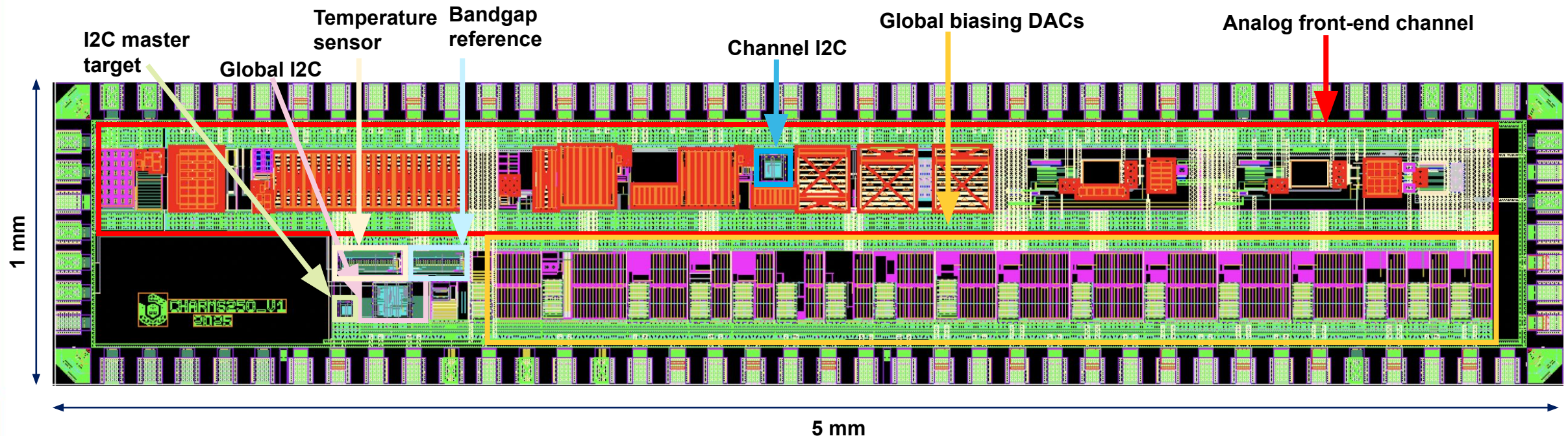
Test structures currently being characterized

Thick-oxide NMOS
($L = 400 \text{ nm}$, $W = 24 \text{ mm}$)

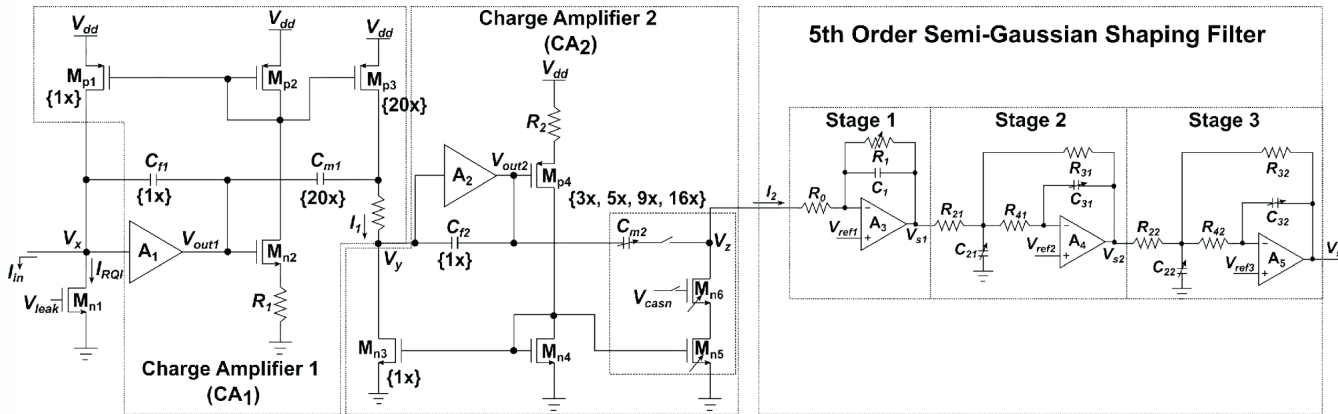
Thick-oxide PMOS
($L = 400 \text{ nm}$, $W = 24 \text{ mm}$)

CHARMS250 ASIC status

- **Prototype CHARMS250 chip (single channel)** to be submitted for fabrication on June 18th
- Preliminary GDS submitted – initial DRC report received (design is DRC clean except for a few density errors, which can be waived)
- **Next steps:**
 - IR drop analysis with Voltus (currently being performed)
 - Completing the documentation
 - Design of 16-channel CHARMS250 complete
 - Design of fast CHARMS (~10 ns shortest peaking time) underway

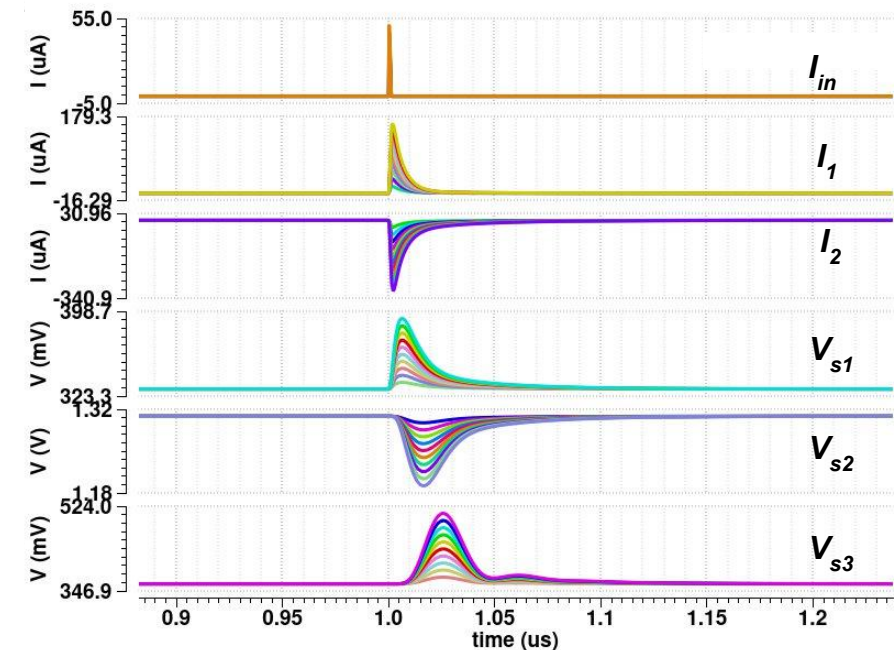


CHARMS10 design ($10 \text{ ns} \leq T_p \leq 250 \text{ ns}$)



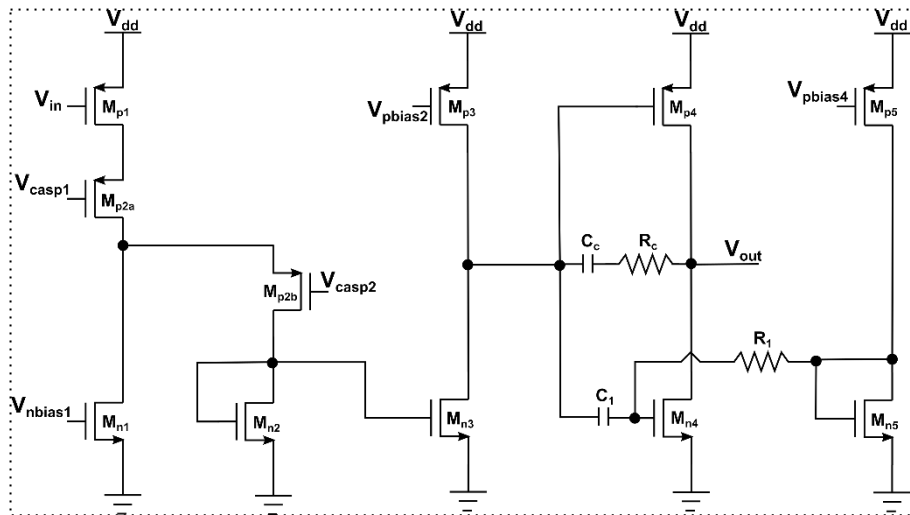
- Limited bandwidth of A_1 and A_2 disallows shaping times $< 250 \text{ ns}$
- Slow response leads to degradation of linearity

Transient response for variable input charge (50 fC – 300 fC) with A_1 and A_2 modeled as ideal VCVS



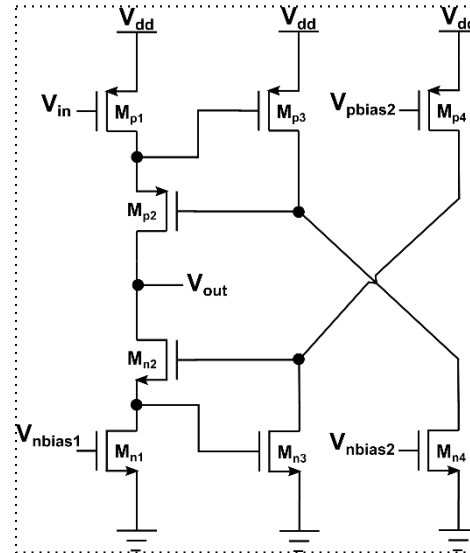
Possible front-end amplifiers for CHARMS10

[1] 3-stage inverting amplifier



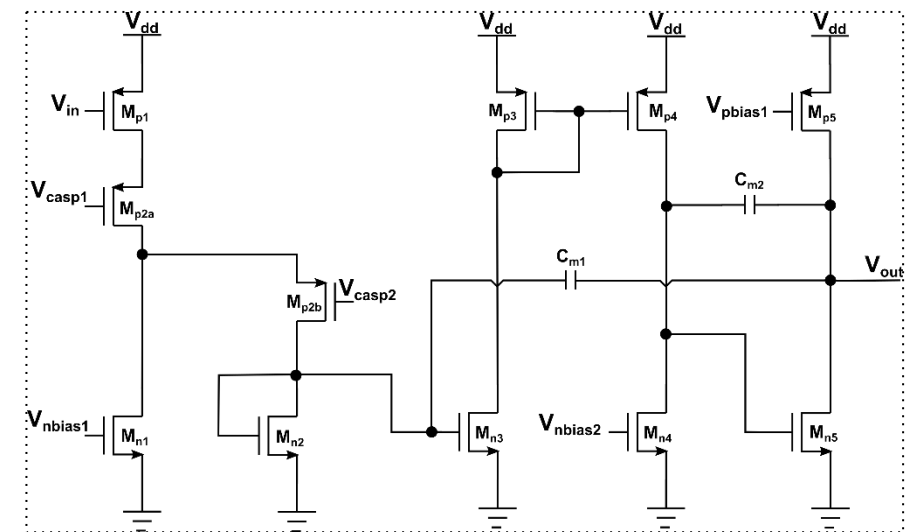
- High open loop DC gain (> 100 dB)
- Same as CHARMS250, works with existing current-mirror based feedback network
- Difficult to achieve higher bandwidth without sacrificing stability

[2] 1-stage inverting amplifier



- Self-cascode gain-boosted amplifier - also possible to achieve high open loop DC gain (~ 100 dB)
- Has a single dominant pole at output node – performance with expected load needs to be analyzed
- Works with existing current-mirror based feedback network

[3] 3-stage non-inverting amplifier



- High open loop DC gain (> 100 dB), high gain-bandwidth product
- Can apply nested-Miller compensation
- Would require redesign of feedback and pole-zero cancellation network

Low-Power Data Links for Stitched Pixel Sensors

What is the Electron-Ion Collider (EIC)?

What is the EIC:

A high luminosity ($10^{33} - 10^{34} \text{ cm}^{-2}\text{s}^{-1}$) polarized electron proton / ion collider with $\sqrt{s}_{ep} = 28 - 140 \text{ GeV}$

What is special:

EIC is the ONLY new collider in foreseeable future.
Allows to remain at frontier of Accelerator S&T.

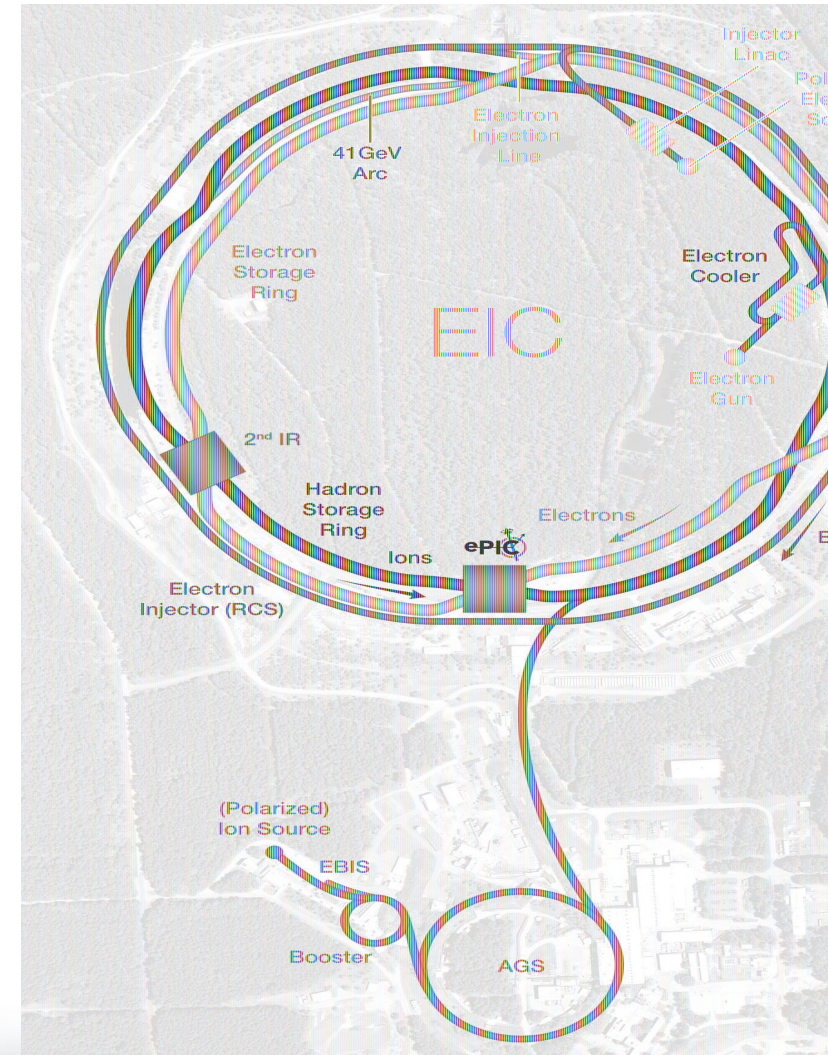
factor 100 to 1000 higher luminosity as HERA
both electrons and protons / light nuclei polarized,
nuclear beams: d to U

Fixed Target Facilities i.e.:

at minimum > 2 decades increase in kinematic
coverage in x and Q^2

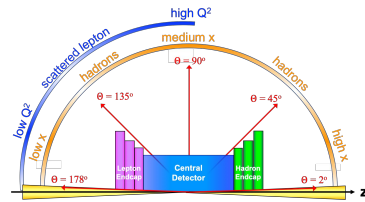
Science Program: An EIC can uniquely address
profound questions about nucleons — neutrons and
protons — and how they are assembled to form the
nuclei of atoms:

State of the art general purpose collider detector



Scope of the Experimental Equipment

- High Luminosity: $L = 10^{33} - 10^{34} \text{ cm}^{-2} \text{ sec}^{-1}$,
10 – 100 fb⁻¹/year
- Highly Polarized Beams: 70%
 - requires high precision electron and hadron polarimetry
- Large Center of Mass Energy Range:
 $E_{\text{cm}} = 29 - 140 \text{ GeV}$
 - Large Detector Acceptance
- Asymmetric beam energies
 - require an asymmetric detector Barrel with electron and hadron endcap 9.5 m



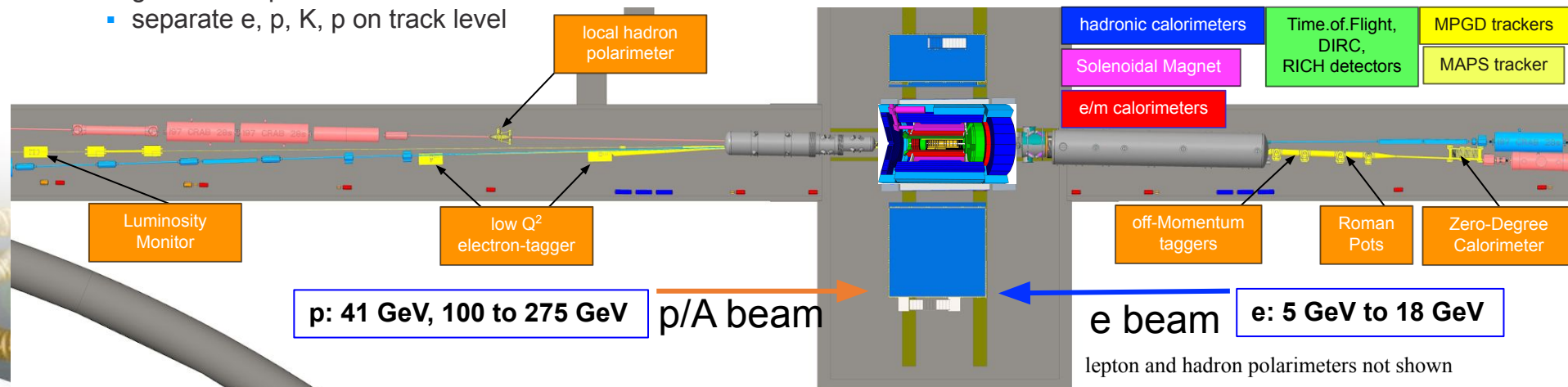
- equal coverage ($-4 < \eta < 4$) Tracking, particle identification, electromagnetic and hadronic calorimetry
 - High precision low mass tracking
 - good e/h separation critical for scattered electron identification
 - separate e, p, K, p on track level

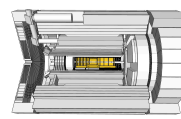
- Science program required momentum resolution
 - requires a large bore ($\varnothing 2.4 \text{ m}$) 2T magnet (1.7 T magnet operation point, stretch goal 2T)
- Imaging science program Large Ion Species Range: protons – Uranium
 - requires specialized detectors integrated in the Interaction Region over 80 m
- Streaming readout electronics model
 - highest scientific flexibility
- very compact Detector Integration is key
- Good Background Conditions

For details see:

https://indico.bnl.gov/event/20473/contributions/85389/attachments/51976/88992/eca.EIC_Background.ePIC.pptx

↪ 25 different Subsystems incl. Polarimetry





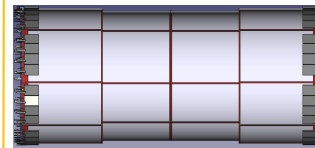
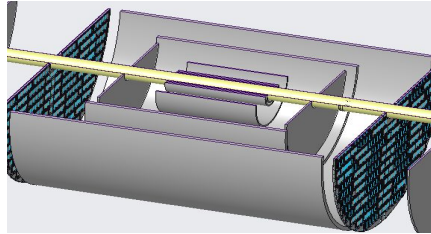
ePIC Tracking Detectors

μ Vertex Tracker

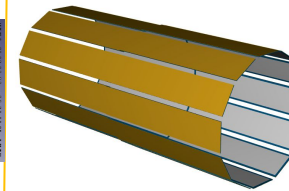
Barrel Tracker

Outer Barrel MPGD Tracker

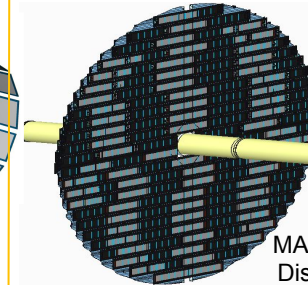
EndcapTracker



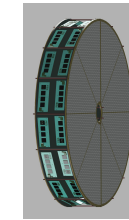
MicroMega Tracker



μ RWELL Tracker



MAPS Disks



μ RWELL Disks

Main Function

Excellent momentum
 $0.05\% p_T \oplus 0.5\%$
and spatial resolution
 $20\mu\text{m}/p_T \oplus 5\mu\text{m}$

Displaced vertex
reconstruction

Tracking layer close to
DIRC detector $\square$
improved angular and
space point resolution.
Redundancy and
pattern recognition for
tracking

Provide redundancy
and pattern
recognition for
tracking

Excellent momentum
 $0.05 (0.10)\% p_T \oplus 1.0$
 $(2.0)\%$
and spatial resolution
 $30\mu\text{m}/p_T \oplus (20 - 40) \mu\text{m}$

Provide redundancy
and pattern
recognition for
tracking

Monolithic Active Pixel
Sensor $\square$ ALICE ITS3
MOSAIX sensor (65 nm),
small pixels ($\sim 18 \mu\text{m}$) and
power consumption (< 20
 mW/cm^2)

Proven Technology

Cylindrical resistive
Micromegas technology
Used: ATLAS NSW,
CLAS12, SPHENIX,
MINOS& T2K TPC

world's first at ePIC

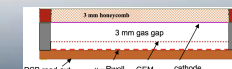
EIC Large Area
Sensor (LAS),
modification of ITS3
sensor with 5 or 6
RSU forming staves
as the basic building
elements for the
Outer Barrel



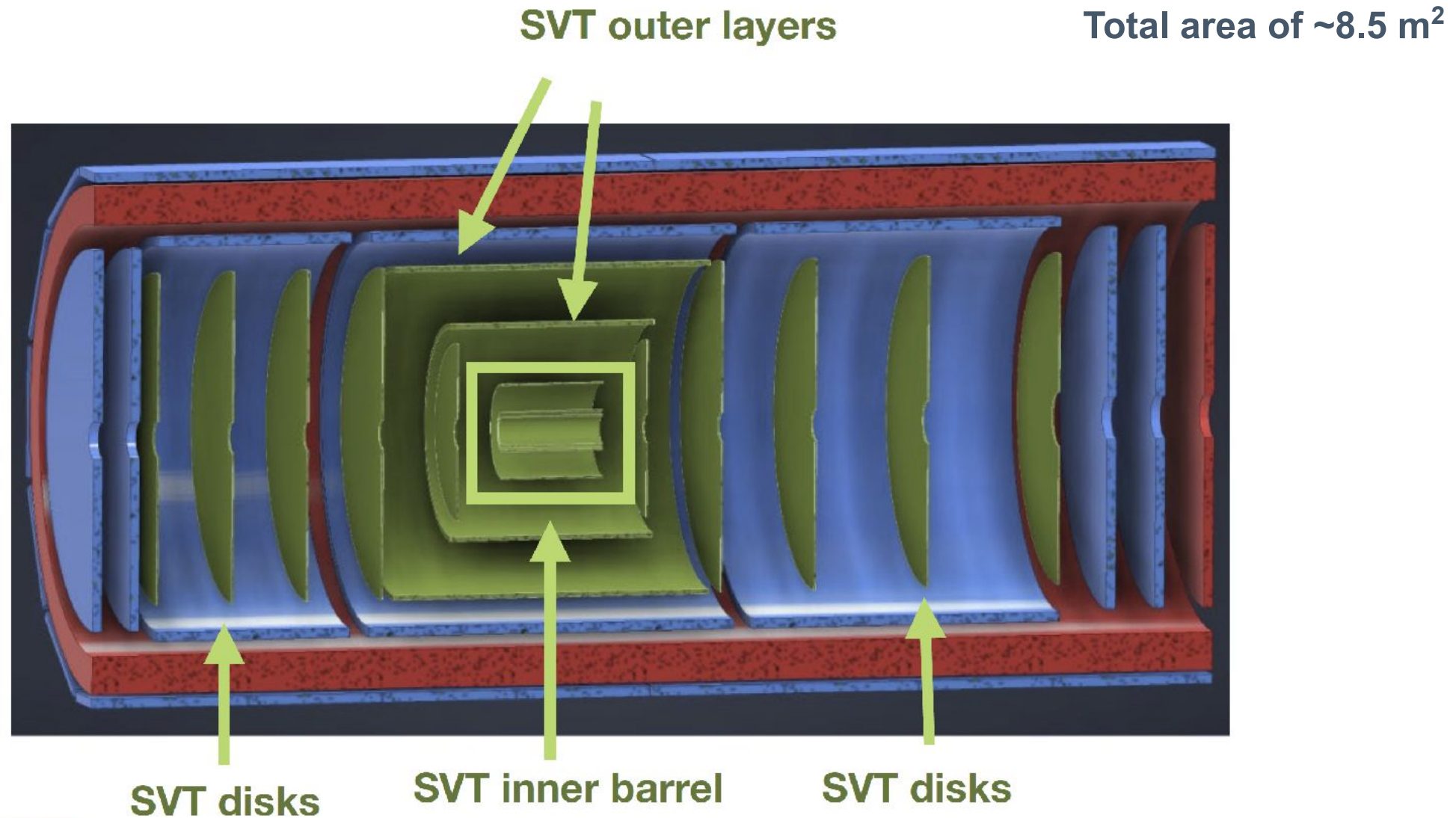
24 planar Thin-gap &
double amplification
(GEM & μ RWELL)
modules &
2D-strip readout

EIC Large Area
Sensor (LAS), staves
as the basic building
elements for the
MAPS disks

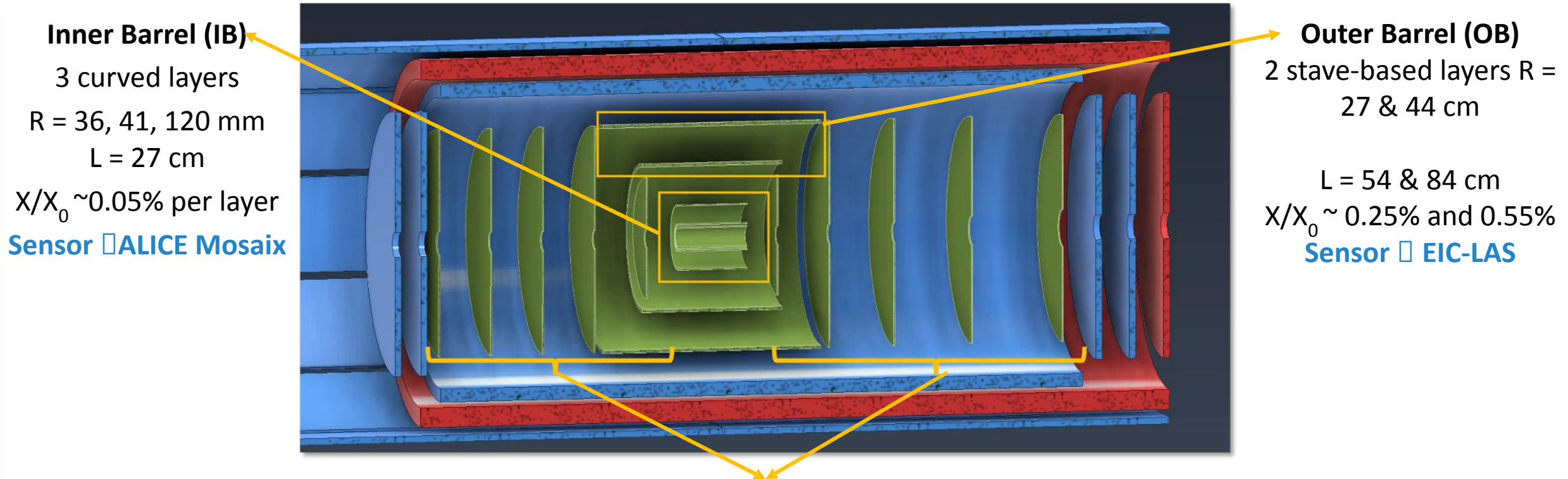
GEM- μ Rwell hybrid
configuration with
increased gain



Silicon vertex tracker (SVT) for the ePIC detector (in green)



Context: ePIC SVT Concept



Total area $\approx 8 \text{ m}^2$

The ITS3 pixel technology for the SVT

ALICE ITS3 Letter of Intent: [ALICE-PUBLIC-2018-013](#)

ALICE ITS3, [arXiv.2105.13000](#)

ALICE ITS3, [arXiv.2212.08621](#)

ITS3: ultra-light (“massless”) sensors with $<0.05 X_0$

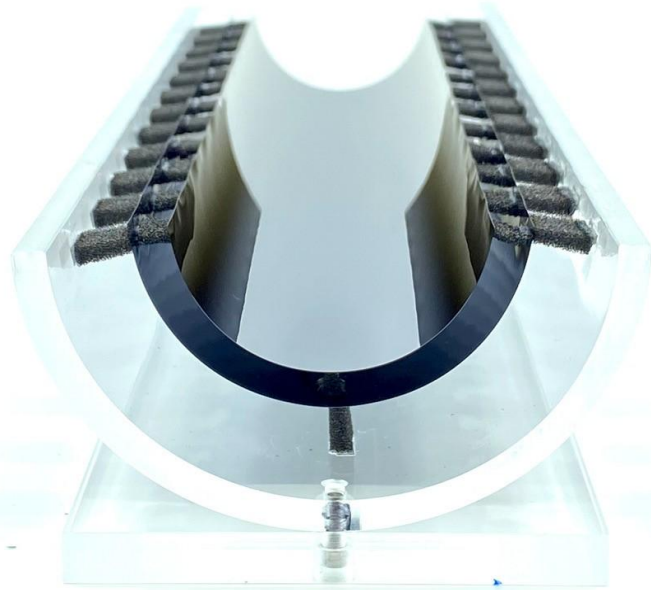
- Large area sensors (LAS) fabricated using reticle stitching
- **Bendable** when thinned below $\sim 20\text{-}40\text{ }\mu\text{m}$

→ Impact parameter resolution of a few μm for $p_T \sim 1\text{ GeV}$

ITS3 fulfills ePIC requirements in terms of spacial resolution and material budget:

→ **Challenge:** ePIC has stronger requirements in terms of integration time!

L. Tomasek, G. M.
Innocenti



ALICE collaboration. *Technical Design report for the ALICE Inner Tracking System 3-ITS3; A bent wafer-scale monolithic pixel detector.* No. CERN-LHCC-2024-003. 2024.

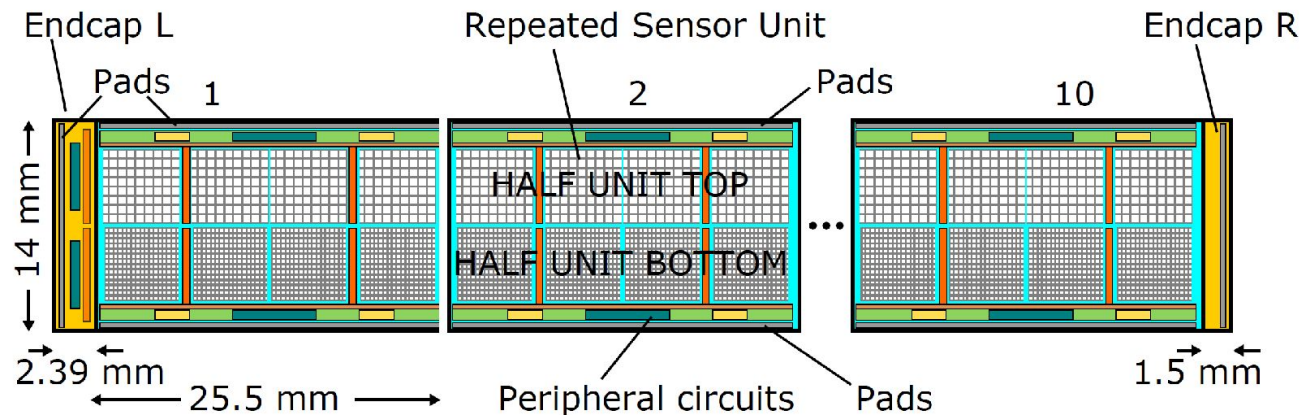


Figure 3.11: Concept diagram of the MOSS chip.

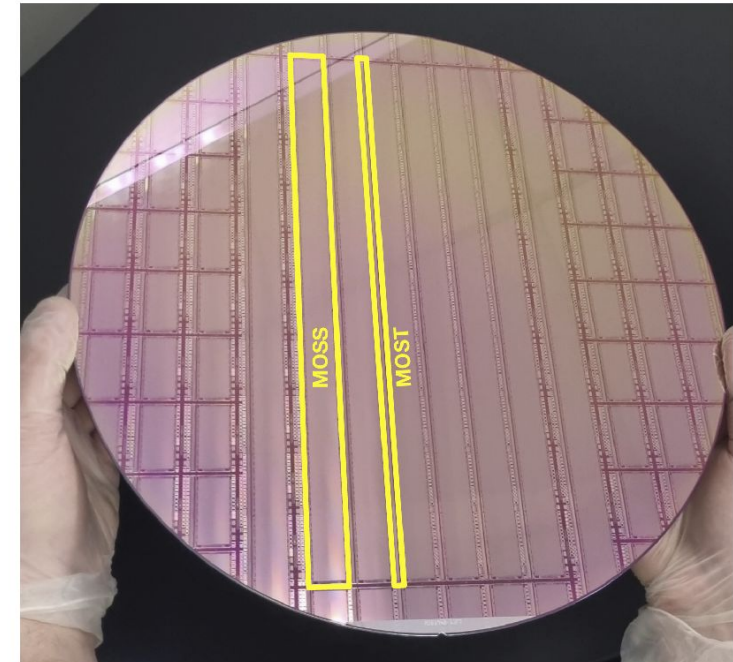
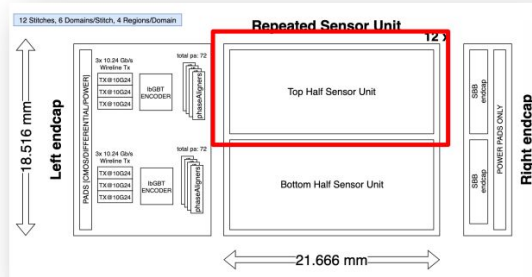


Figure 3.25: A 300mm ER1 wafer, containing six MOSS and MOST stitched sensors (indicated), as well as a number of small prototype chips.

Introduction: On-chip links for ALICE ITS3 MAPS

- **Goal:** Transmit data across the stitched large area sensor (~20 cm) at 160 Mb/s
- Would like to avoid the use of repeaters at boundaries
- High resistivity and capacitance density of the metal layers severely limit the bandwidth of long-range wired links across the sensor



Each Half Unit is segmented in Powering **Domains**

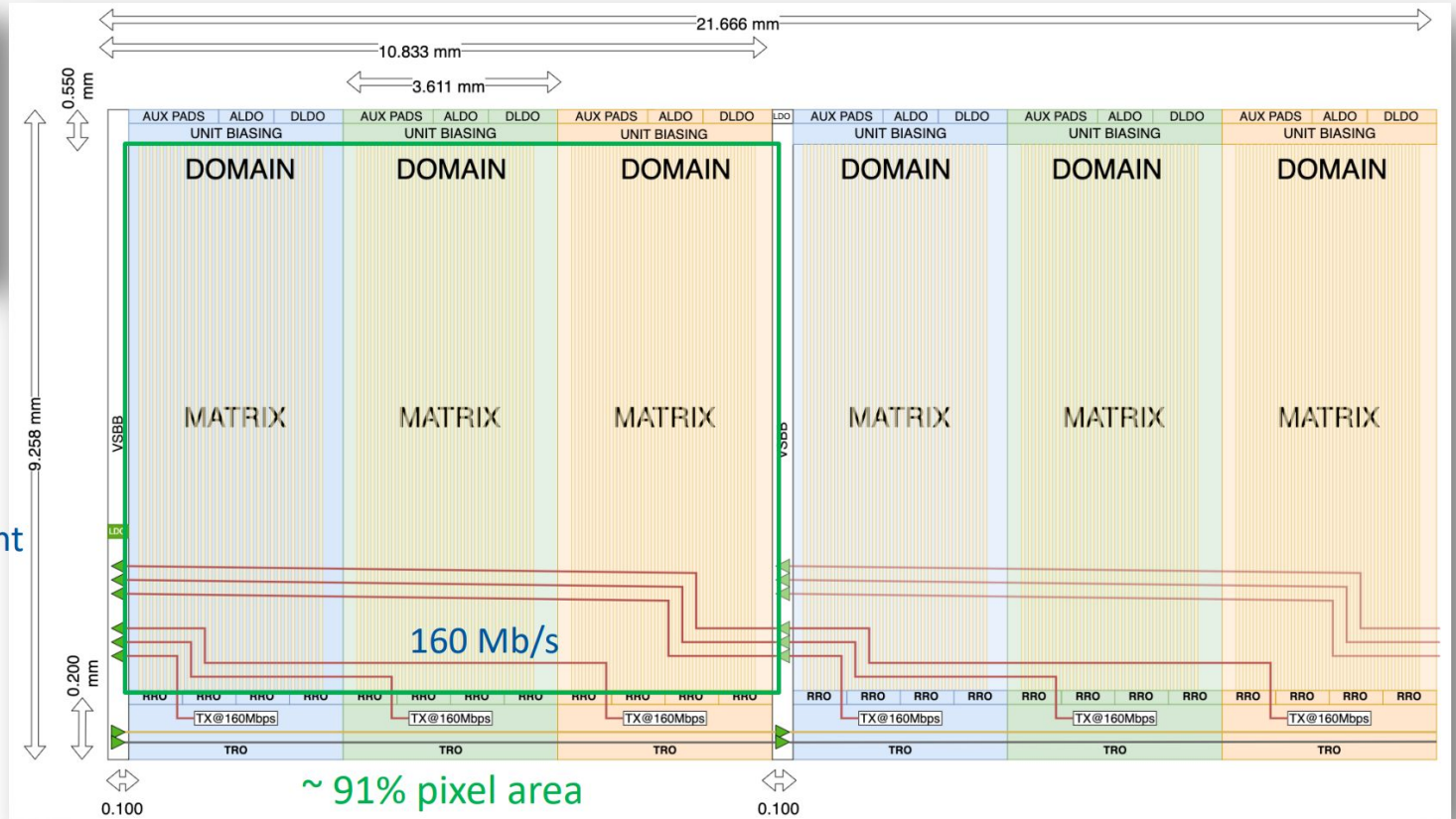
Each Domain acts as independent pixel sensor

Powering

Biassing

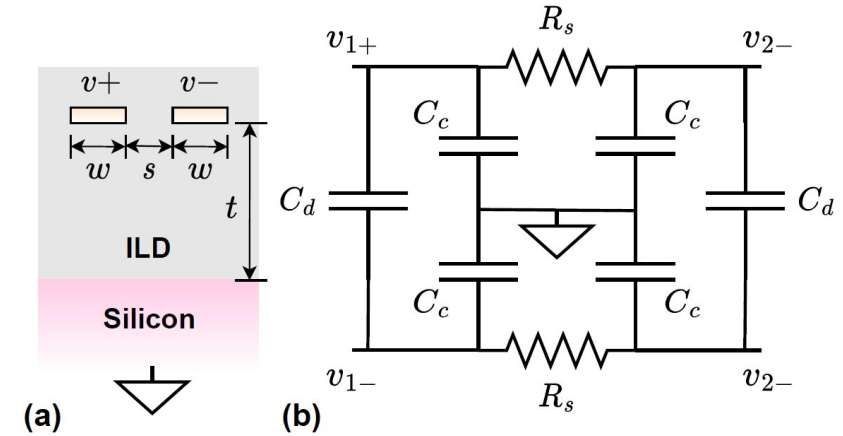
Configuration

Readout Link (160 Mb/s)



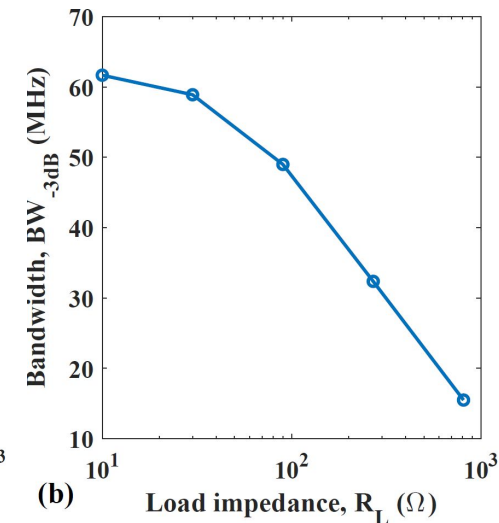
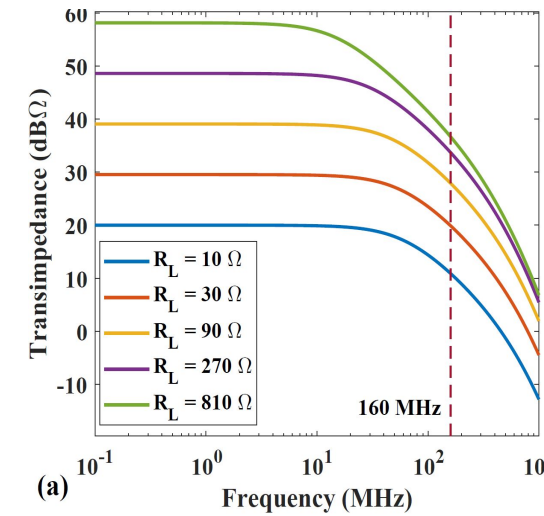
Proposed Power-Efficient Link Design

- **Initial design:** differential microstrip on top metal layer
 - The top layer (Metal 6) has a sheet resistance of $40 \text{ m}\Omega/\square$ and is located about $\approx 4 \text{ }\mu\text{m}$ above the substrate
 - Design parameters: width (w), spacing (s) and vertical separation from the substrate
 - Frequency is low enough for inductance to be ignored: line can be approximated by distributed RC network
 - Bandwidth, $\text{BW} \approx 0.5/(2\pi RC)$, tends to increase with w due to reduced fringe capacitance



- **Transimpedance gain:** link $L = 10 \text{ cm}$ (M6), $w = 5 \text{ }\mu\text{m}$ and $s = 1 \text{ }\mu\text{m}$
 - Effective link bandwidth is defined by the frequency response of the line transimpedance:

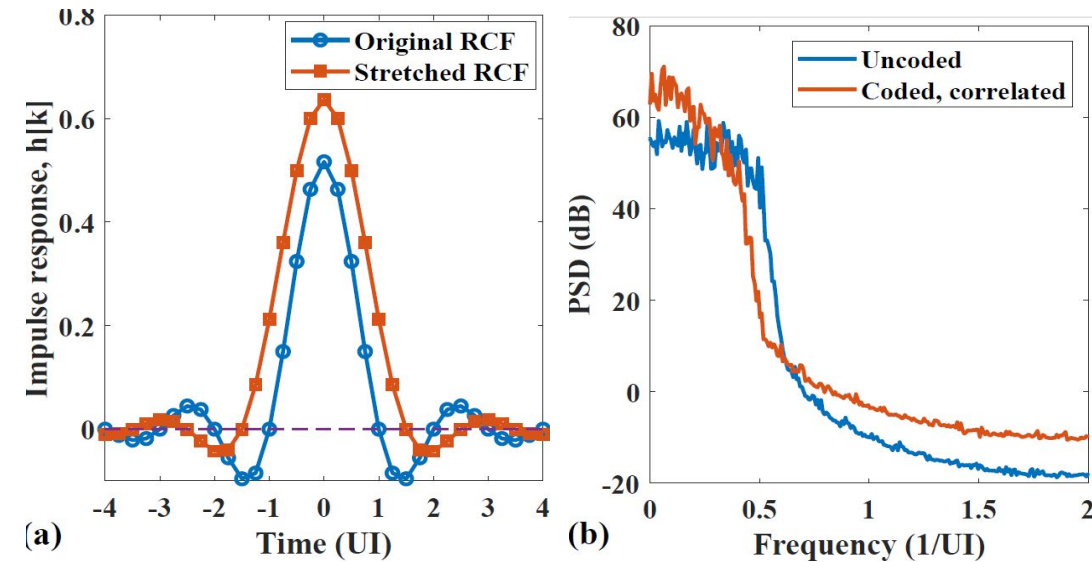
$$Z_T(\omega) = V_{RX}(\omega)/I_{TX}(\omega)$$
 - Low-frequency value of $|Z_T(\omega)|$ increases with R_L
 - Bandwidth also decreases, which reduces channel capacity and, thus, the maximum achievable data rate
 - The bandwidth decreases by approximately 4x as R_L varies over two orders of magnitude
 - Time constants decrease along with R_L



Proposed Power-Efficient Link Design: Line Coding

- Correlative level coding (CLC) is considered for line coding
- The line coding process operates in two steps
 - First step:** Duobinary encoding for generating correlations, summarized by:
 - If $x[n] = 0$, $y[n - b + 2 : n]$ has an even number of '1's
 - If $x[n] = 1$, $y[n - b + 2 : n]$ has an odd number of '1's
 - Second step:** Pulse shaping for zero ISI, summarized by:

$$h(nT_s) = \begin{cases} 1, & n = 0 \\ 0, & \text{otherwise} \end{cases}$$



- Typical link designs use a raised cosine filter (RCF) for pulse shaping. The impulse response of an RCF is zero at the center of each symbol ($h[k] = 0$ for $k = nM$, n is an integer)
- The key idea for CLC is to modify the pulse shaping function such that a controlled amount of ISI is intentionally introduced between adjacent symbols. The shaping function used for duobinary signaling is

$$h[k] = \frac{2}{\pi T_s} \left[\frac{\cos(\pi k/M)}{1 - 4(k/M)^2} \right]$$

- The result is a stretched version of the RCF with a low-pass frequency response of the form $H(\omega) = \cos(\omega T_s/2)$, which goes to zero smoothly at $\omega = \pi/T_s$
- The power spectra of random binary data comparison for standard RCF and stretched RCF shows that
 - sidelobes in both scenarios are completely eliminated;
 - the bandwidth of the main lobe is reduced by $\sim 20\%$, relaxing channel bandwidth requirements for a given data rate

Proposed Power-Efficient Link Design: Line Coding

Key Takeaway Point:

Instead of sending raw square waves, our datalink design prioritizes the transmission of carefully shaped waveforms and encoded symbol streams for optimized bandwidth usage, signal integrity, and DC balance

John, Nicholas St, et al. "Self-Adaptation of Line Driver Pre-Emphasis Parameters via Embedded Line Loss Sensing." *2023 18th Conference on Ph. D Research in Microelectronics and Electronics (PRIME)*. IEEE, 2023.

John, N. St, et al. "A low-power 1 Gb/s line driver with configurable pre-emphasis for lossy transmission lines." *Journal of Instrumentation* 18.04 (2023): C04009.

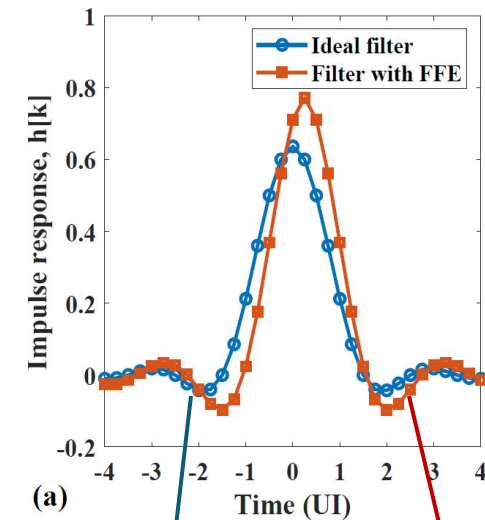
John, Nicholas St, et al. "Testing of a line driver with configurable pre-emphasis on lossy transmission lines." *IEEE Transactions on Nuclear Science* (2024).

Proposed Power-Efficient Link Design: Line Coding

- The resulting eye diagrams for standard RCF and stretched RCF are obtained for the typical value of $f_c = 1/(3*UI)$, i.e., 53.33 MHz for the nominal data rate of 160 Mb/s
- Standard RCF shows the usual binary eye diagram; however, the stretched RCF exhibits ternary eye diagrams
- Both the coded and uncoded eye diagrams exhibit a moderate amount of ISI due to finite channel bandwidth
- To remove the ISI, the shaping function can be modified as

$$H'(\omega) = \frac{H(\omega)}{H_c(\omega)}$$

- The inclusion of $H_c(\omega)$ in the shaping function can be viewed as **pre-emphasis or feed-forward equalization (FFE)**
- It is interesting to compare the impulse responses of the ideal duobinary and modified shaping filter
- A first-order lowpass response is an adequate approximation for $H_c(\omega)$ since it only has to capture the line response over the limited bandwidth of the original shaping filter, $H(\omega)$
- **Result:** ISI is completely cancelled at the sampling instants



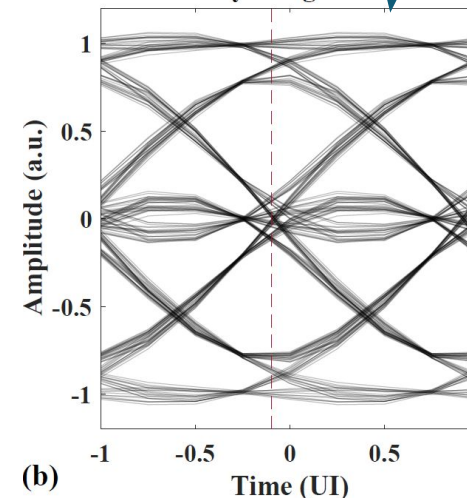
(a)

Standard RCF

Modified RCF + CLC

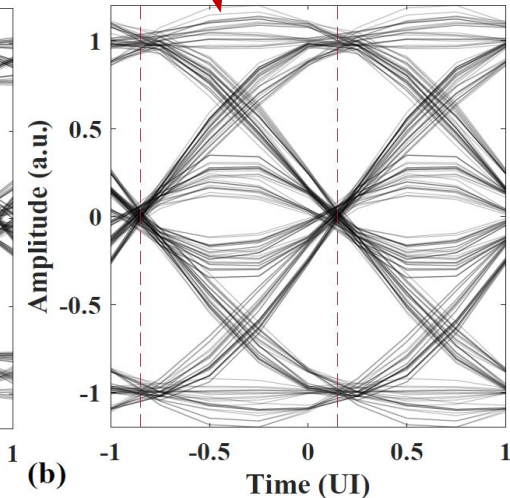
Eye diagram

Eye diagram



(b)

Time (UI)



(b)

Time (UI)

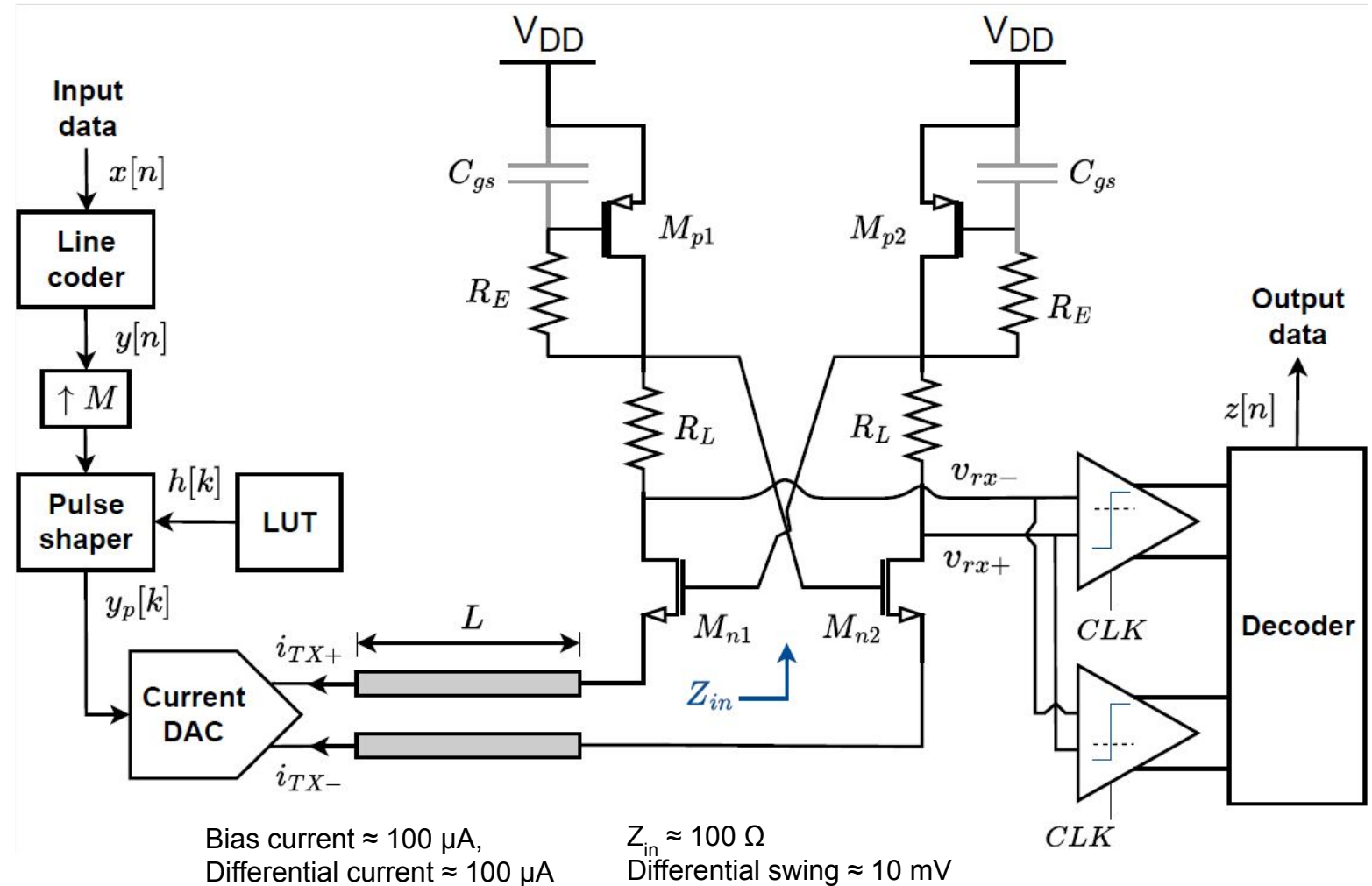
Proposed Power-Efficient Link Design: Line Coding

Key takeaway point:

Correlative Level Coding effectively mitigates ISI caused by limited channel bandwidth, though with a degree of high-frequency noise amplification. The link also requires pre-emphasis filtering in the transmitter and a multi-level discriminator in the receiver.

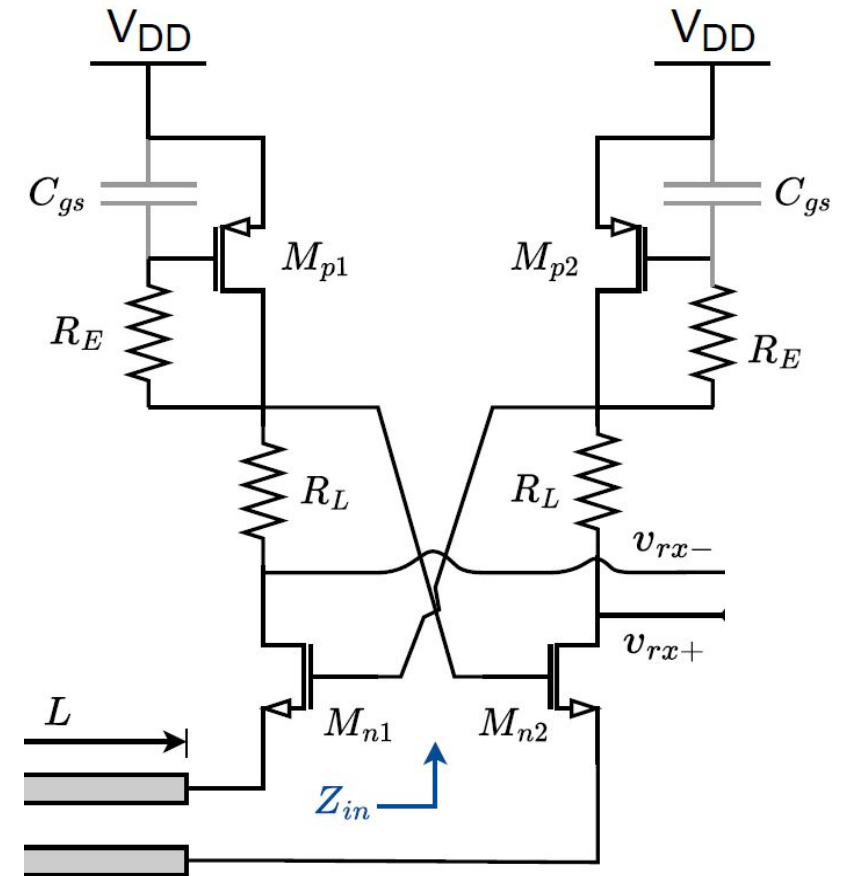
Implementation of the entire link

- The previously mentioned CLC and FFE procedures are incorporated in the proposed link, which was designed for lengths up to $L = 20$ cm
- The transmitter uses synthesized digital blocks for the line coder, upsampler, and pulse shaper, which forms a simplified FIR filter
- The output of the FIR filter is converted into differential current by a current DAC through 2^N matched differential current cells
- The DAC also includes a pair of single-ended cells that generate a common-mode output current, I_{CM}
- This DC current is used to reduce the fractional change in bias current for the TIA in the receiver, thus improving its linearity



Transimpedance amplifier (TIA)

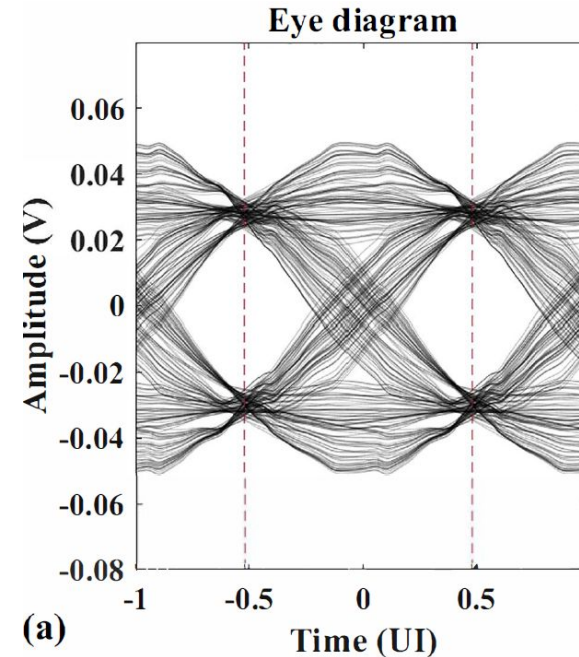
- The goal is to minimize the input impedance of the TIA, $|Z_{in}|$, to maximize channel bandwidth
- At the same time, the transimpedance of the TIA should be maximized to ensure nearly flat Z_{in} over the signal bandwidth
- The chosen design decouples these quantities by using the cross-coupled pair of PMOS transistors (M_{p1} and M_{p2}) to provide a controlled amount of positive feedback
- The input impedance decreases from $1/g_{mn}$, where g_{mn} is the transconductance of the input NMOS pair (M_{n1} and M_{n2}). Device sizing is used to ensure that $g_{mp} > g_{mn}$, which is necessary for stability ($\text{Re}(Z_{in}) > 0$)
- The resistance R_E combines with the parasitic C_{gs} of the PMOS pair to realize an active inductance of value $R_E C_{gs}/g_{mp}$



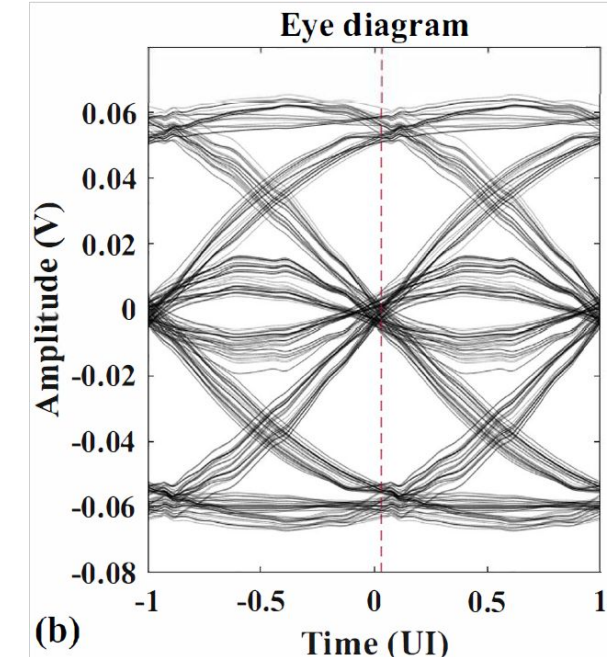
$$Z_{in} \approx \frac{1}{g_{mn}} - \frac{1}{g_{mp}} \quad Z_{rx} \approx R_L + \frac{1}{g_{mp}}$$

Transimpedance amplifier (TIA)

- The proposed link was implemented at the transistor level using Cadence Virtuoso
- The nominal TIA input impedance is $Z_{in} \approx 100 \Omega$ at low frequencies, resulting in an estimated -3 dB link bandwidth of ~ 50 MHz ($0.3/\text{UI}$)
- Nevertheless, both eye diagrams are completely open, with nearly perfect ISI cancellation at the sampling instants
- The bandwidth of RC lines scales $\propto 1/L^2$, since both R and C increase $\propto L$, which ultimately limits the maximum usable line length



Without duobinary coding



With duobinary coding

Differential comparator

- Comparator comprises of two-stage design
 - Resistively loaded differential preamplifier to reduce input-referred noise and offset
 - StrongArm latch with programmable device width (W) for the input transistors to allow input threshold adjustment
 - Width is adjusted by turning on/off parallel branches, each containing a unit transistor and a switch (total of 32 (16+16) identical branches)

- Few key parameters:

- Bias current $I_B = 120 \mu\text{A}$
- Nominal voltage gain of 10 dB
- Load capacitance, $C_L = 85 \text{ fF}$ ($\text{BW} \approx 2.4/\text{UI}$)
- Input-referred thermal noise PSD $6.6 \text{ nV/Hz}^{1/2}$
- $1/f$ corner frequency 4.1 MHz
- Total output voltage noise of $540 \mu\text{V}_{\text{rms}}$
- The total noise across for the entire link

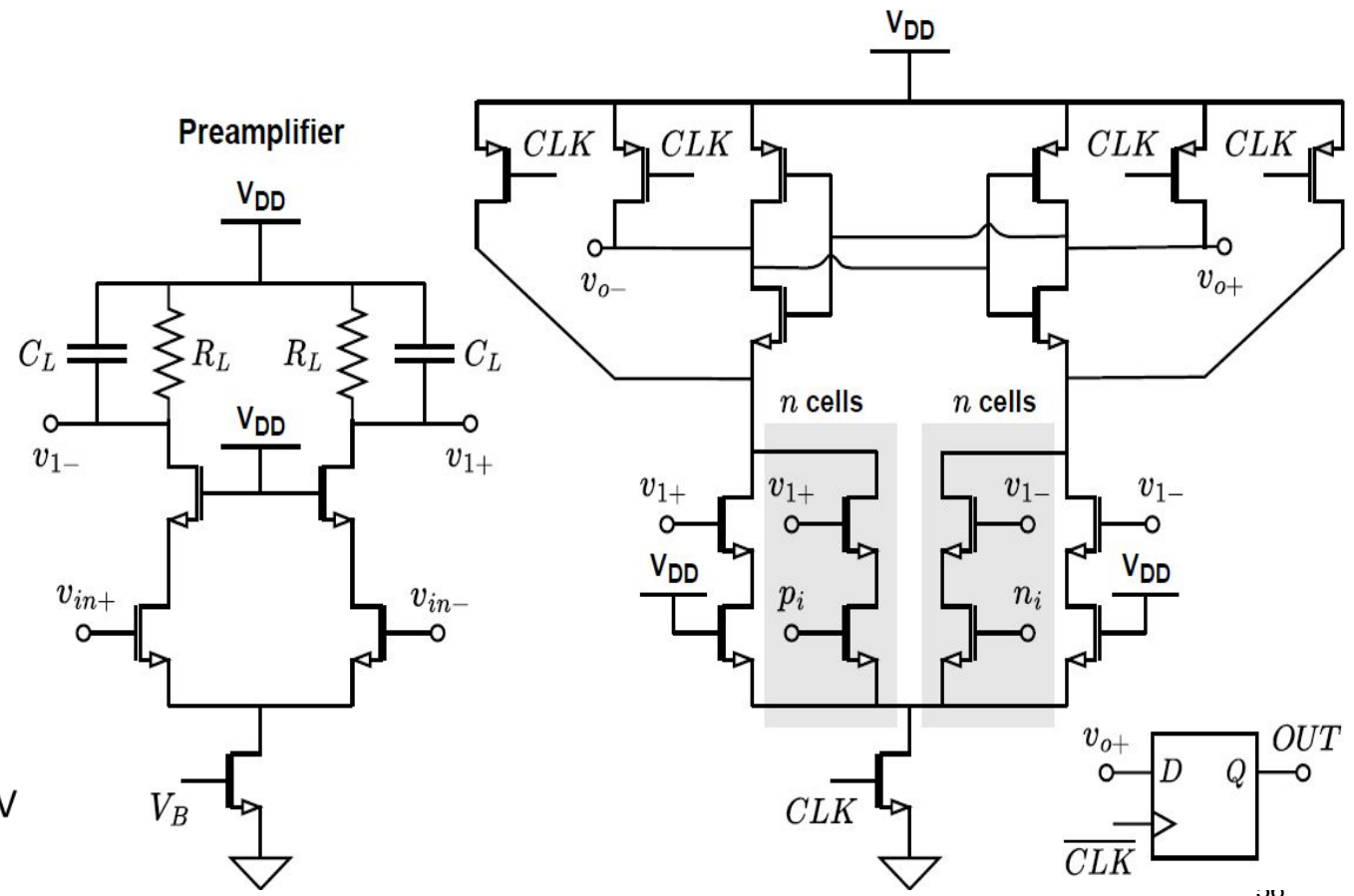
$$\sigma_{n,\text{out}} = 4.9 \text{ mV}_{\text{rms}} \text{ (under noise simulation)}$$

Nominal input transistor size:

$$W = 12.8\mu, \quad L = 0.1\mu$$

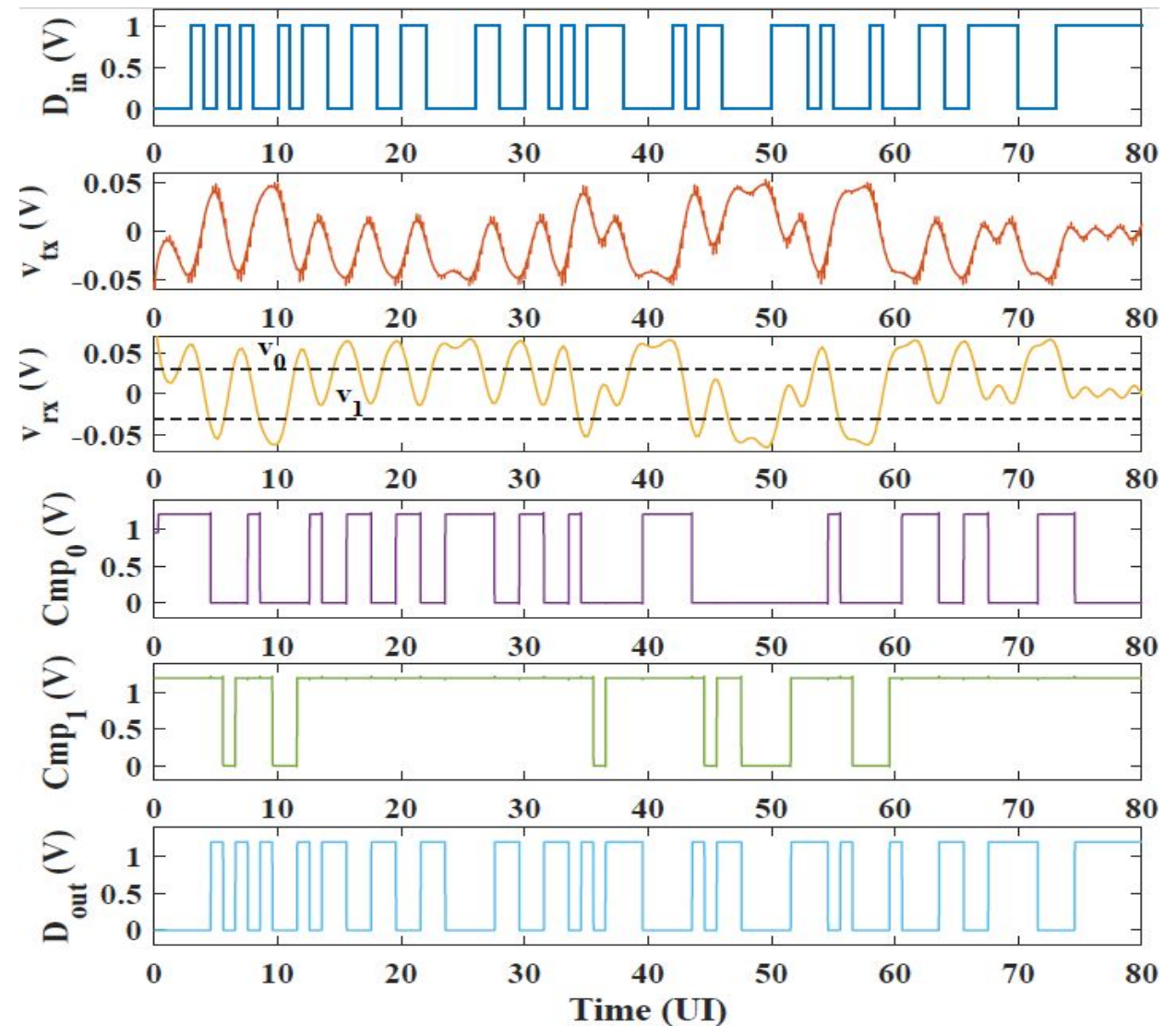
$$\Delta V_T = V_L \frac{\Delta W}{W} \approx 2 \text{ mV}$$

Adding β mismatch, expect $\sigma_{VT} \approx 4.5 \text{ mV}$



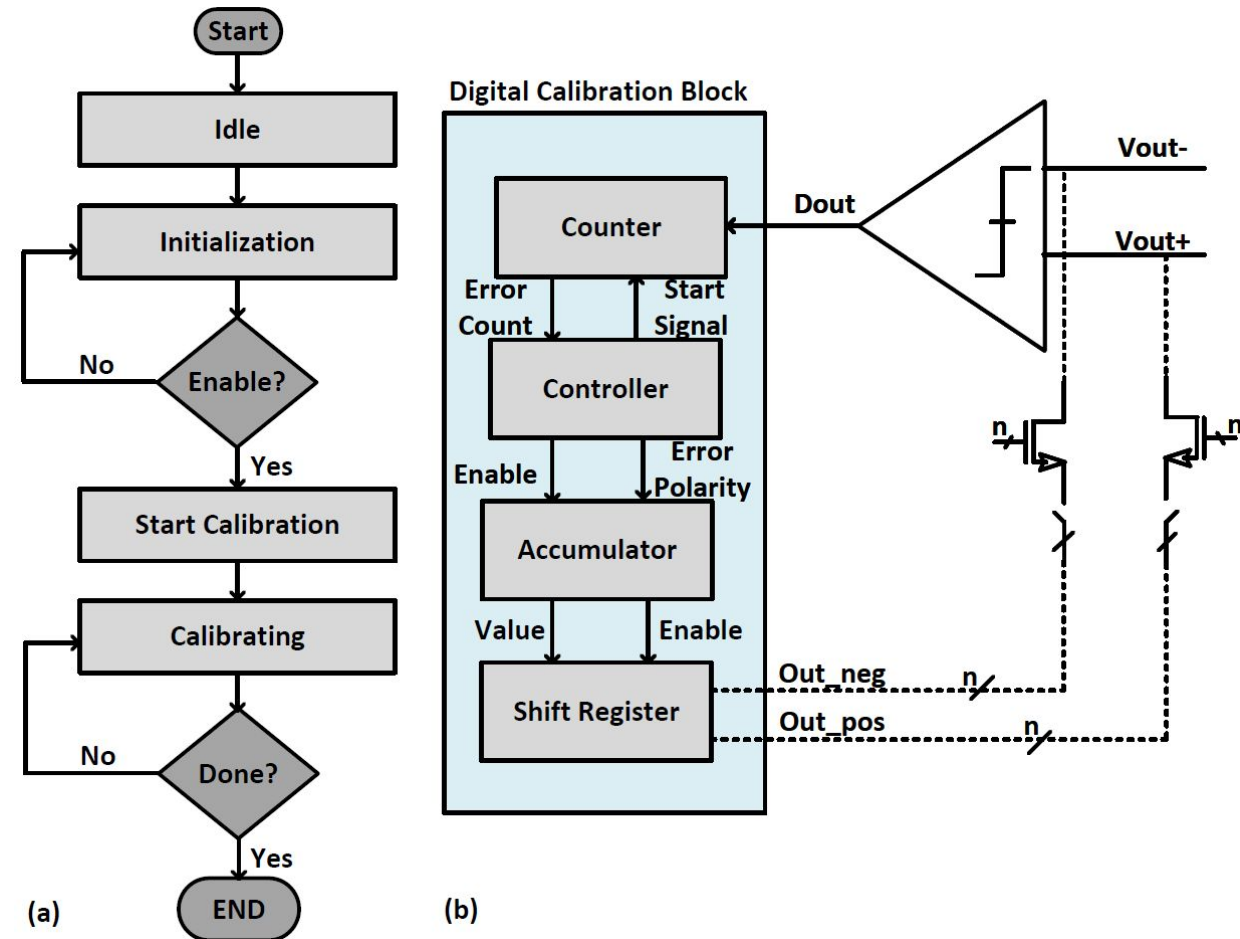
Transient Simulation Result of the Link

- The band-limiting provided by pulse shaping results in nearly perfect transmission of the voltage waveform across the link
- The offset voltages of the two comparators were programmed via the width adjustment mechanism described earlier, resulting in the symmetric slicing levels, v_0 and v_1 , of approximately ± 30 mV
- The estimated noise voltage across the preamplifier outputs is small enough to ensure no measurable bit errors. Thus, the link is not noise-limited
- The simulated power consumption of the entire link was 596 μW , resulting in an excellent FoM of 37.3 fJ/bit/mm for $L = 10$ cm



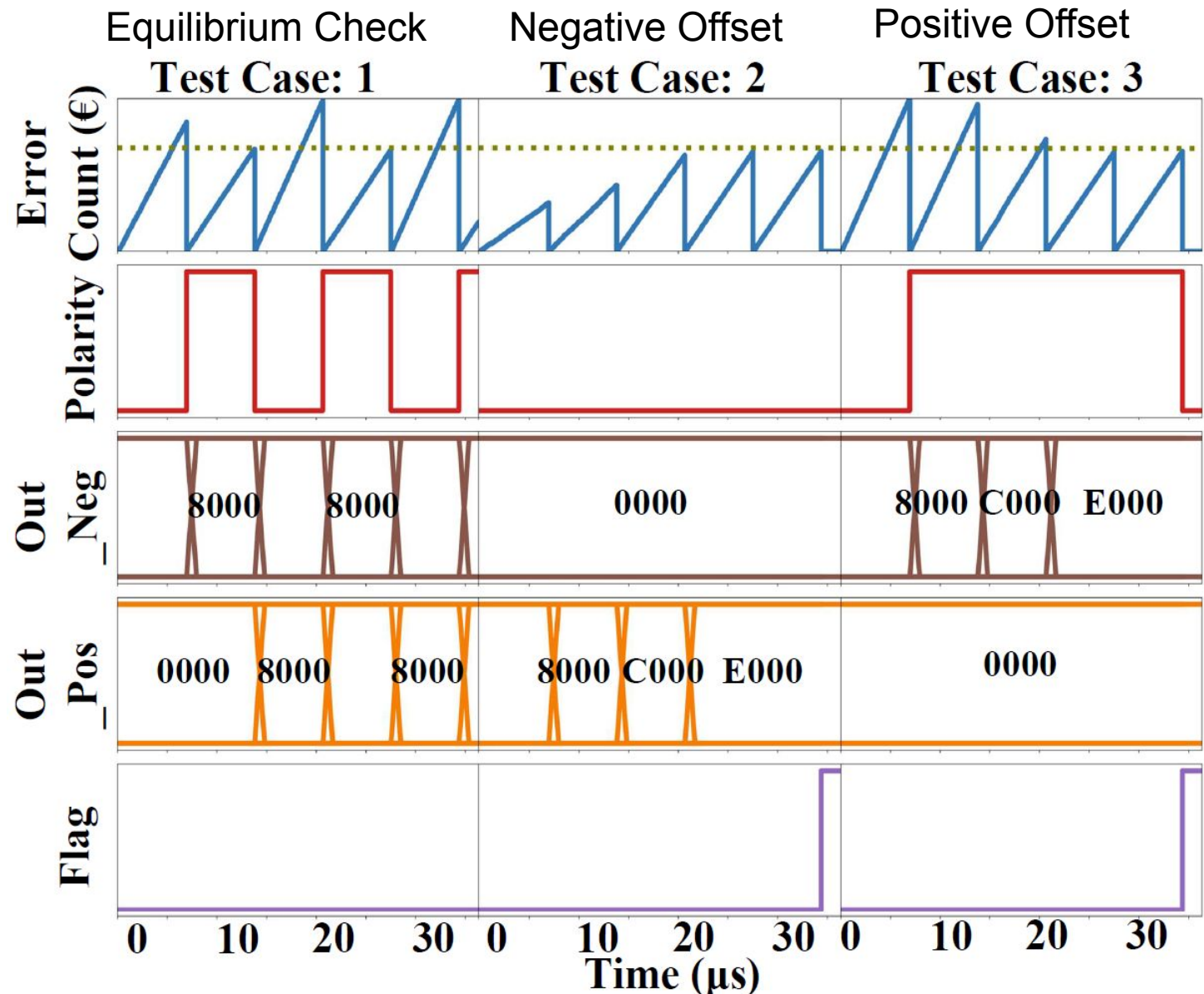
Offset Calibration System

- All-digital calibration technique that provides
 - Programmability
 - Can be run at startup for automated Self-calibration capability
 - Adjustable to provide the intentional offsets to sample ternary received waveforms
- A finite state machine (FSM) controls the calibration technique and comprises four states: *Idle*, *Initialization*, *Calibrating*, and *Complete*
- Digital calibration block contains a counter, controller, accumulator, and shift register
- The FSM accounts for fluctuations due to noisy environments and provides overall system stability
- Area: $3800 \mu\text{m}^2$ (post synthesis with 12T standard cell library)



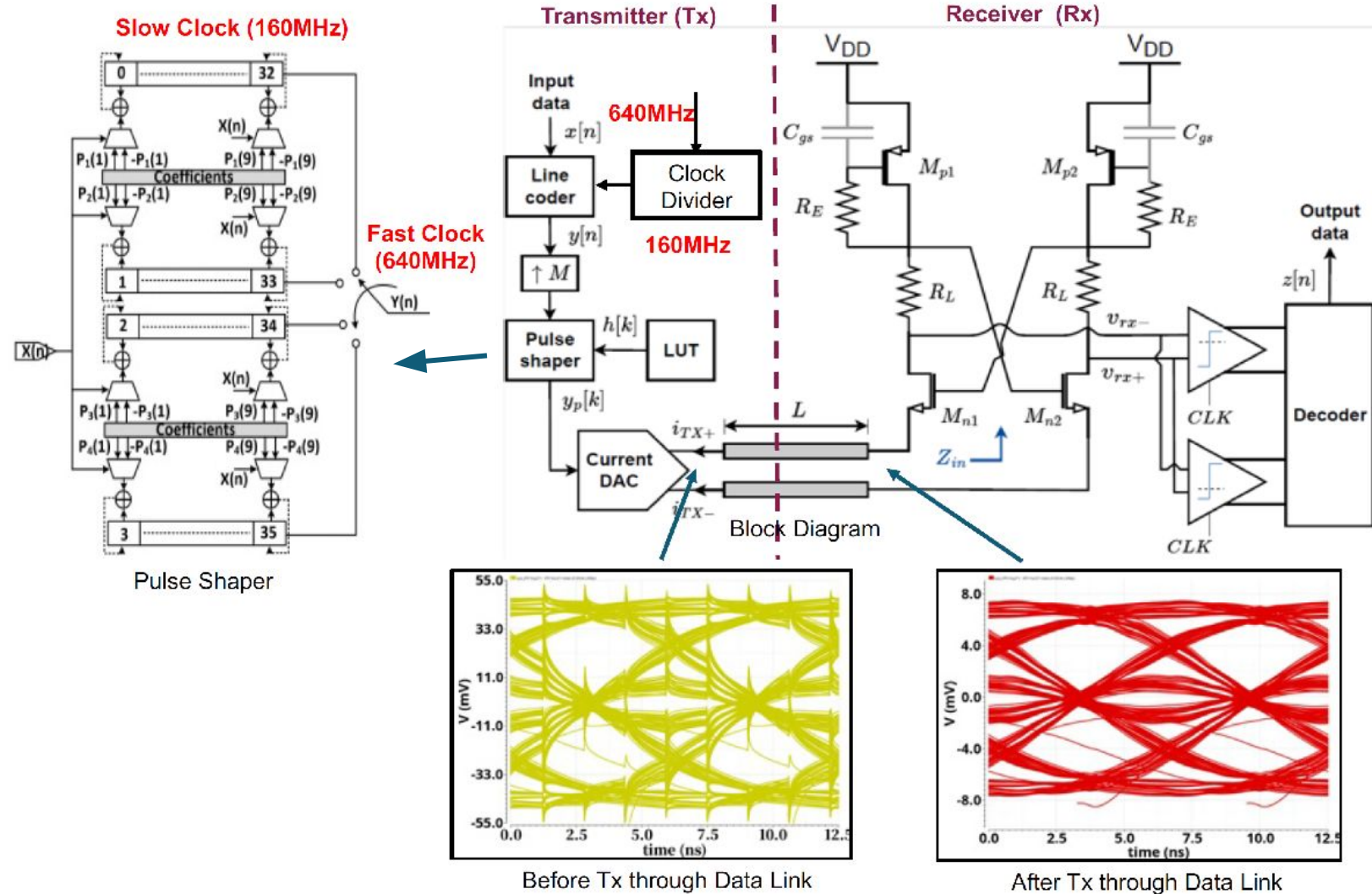
Simulation of Offset Calibration Procedure

- Transient noise simulation of the digital calibration procedure for three different cases at a rate of 160 Mb/s
- The error threshold limit is defined by half of the total counter width. In this case, error count, ϵ , should be around 512 (50% duty cycle) without offset due to 10-bit counter
- **Case 1** runs without any equilibrium check
- Throughout the iterations, incorrect decisions persist leading to a failure in the calibration procedure, and the calibration end flag does not go high for Case 1
- **Case 2** runs on a negative offset and **Case 3** is on a positive offset. Based on the error count being $\epsilon > \epsilon_0$ or $\epsilon < \epsilon_0$, the adjustment is made



Complete implementation

- Key digital transmitter blocks: duobinary line coder, upsampler, and FIR pulse shaper
 - All blocks were synthesized and placed & routed using a standard digital flow
- Pulse shaper has programmable LUT coefficients for flexibility and integrated pre-emphasis
 - Uses a 4x interleaved polyphase structure to reduce power consumption
 - Coefficient quantization was optimized to balance accuracy and hardware efficiency
 - Output drives a unary-coded 6-bit current-steering DAC



Complete implementation (2)

- A complete prototype of the link was implemented in the TPSCo 65 nm CMOS imaging process
- To simplify testing, a 7 cm long “folded” differential Tx line was implemented on-chip
- Estimated figure of merit (FoM) of 37.3 fJ/bit/mm,
 - Comparable to the state-of-the-art for on-chip links

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 53, NO. 3, MARCH 2018

873

A 10-Gb/s/ch, 0.6-pJ/bit/mm Power Scalable Rapid-ON/OFF Transceiver for On-Chip Energy Proportional Interconnects

Da Wei¹, Student Member, IEEE, Tejasvi Anand, Member, IEEE, Guanghua Shu², Member, IEEE, José E. Schutt-Ainé, Fellow, IEEE, and Pavan Kumar Hanumolu, Member, IEEE

ISSCC 2022 / SESSION 28 / DRAM AND INTERFACE / 28.5

28.5 A 0.385-pJ/bit 10-Gb/s TIA-Terminated Di-Code Transceiver with Edge-Delayed Equalization, ECC, and Mismatch Calibration for HBM Interfaces

Hyunsu Park¹, Yoonjae Choi¹, Jincheol Sim¹, Jonghyuck Choi¹, Youngwook Kwon¹, Junyoung Song², Chulwoo Kim¹

A 65-nm 10-Gb/s 10-mm On-Chip Serial Link Featuring a Digital-Intensive Time-Based Decision Feedback Equalizer

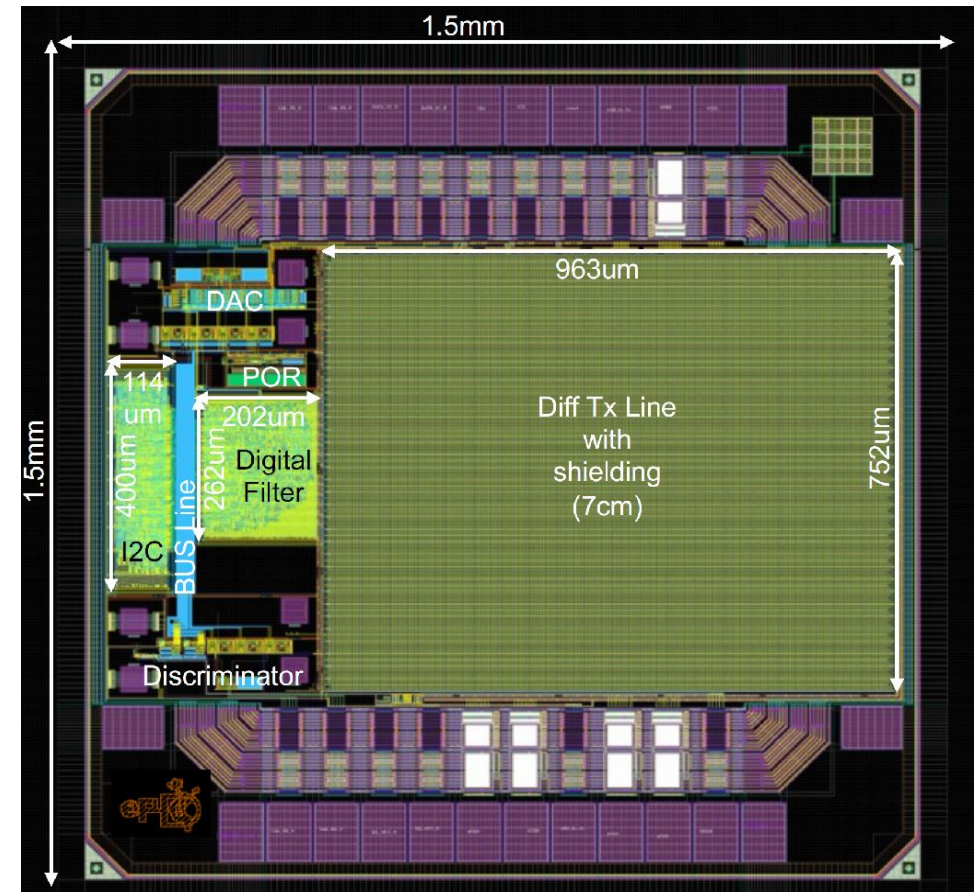
Po-Wei Chiu¹, Somnath Kundu², Member, IEEE, Qianying Tang³, Student Member, IEEE, and Chris H. Kim, Senior Member, IEEE

Best prior FoM:
9.5 fJ/bit/mm at 3 Gb/s



Current-Mode Transceiver for Silicon Interposer Channel

Seung-Hun Lee, Seon-Kyoo Lee, Byungsub Kim, Hong-June Park, and Jae-Yoon Sim, Senior Member, IEEE



Layout of test chip (currently being fabricated)

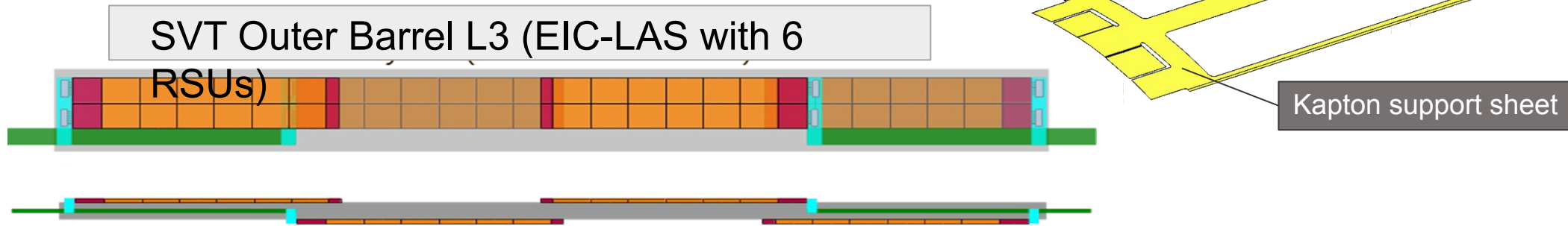
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 9, SEPTEMBER 2014

An Integrated Negative Bias Voltage Generator for Stitched Pixel Sensors

Context: SVT Outer Barrel Module

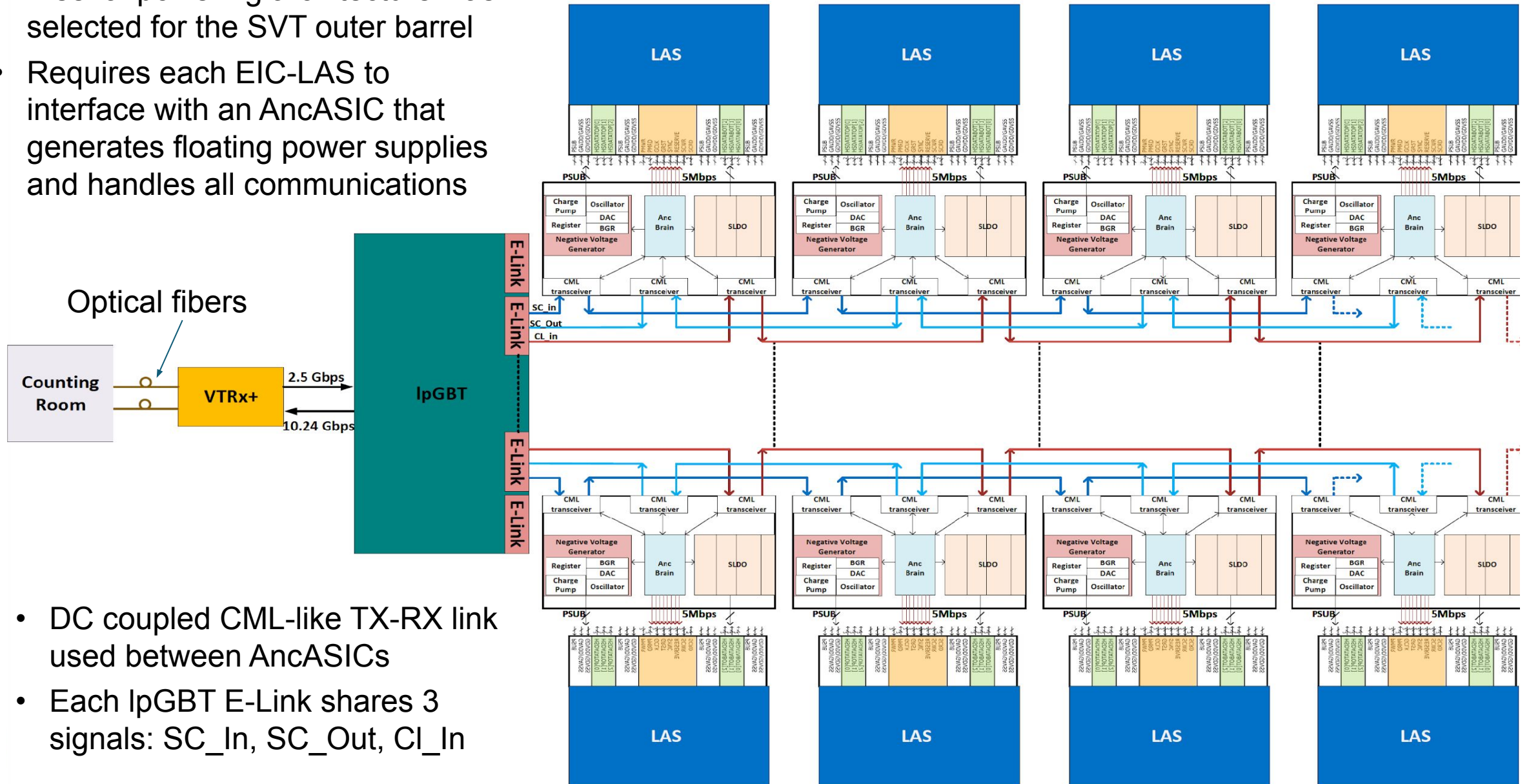
Outer Barrel (Layer3, Layer4)

- Double-sided staves
- Using EIC-LAS (6 RSUs, 5 RSUs)
- 2 EIC-LAS wide (1 module)
- 4 or 8 modules long
- 2 or 4 groups of 4 EIC-LAS (8, 16 total)



Context: Serial powering of EIC-LAS

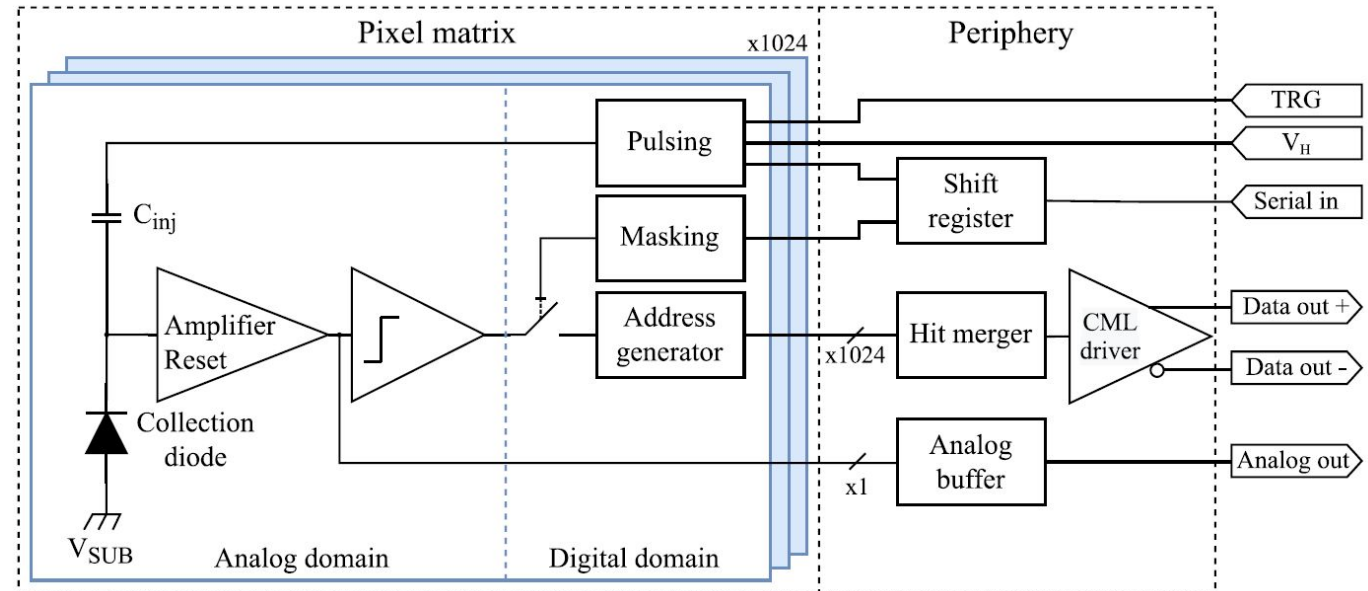
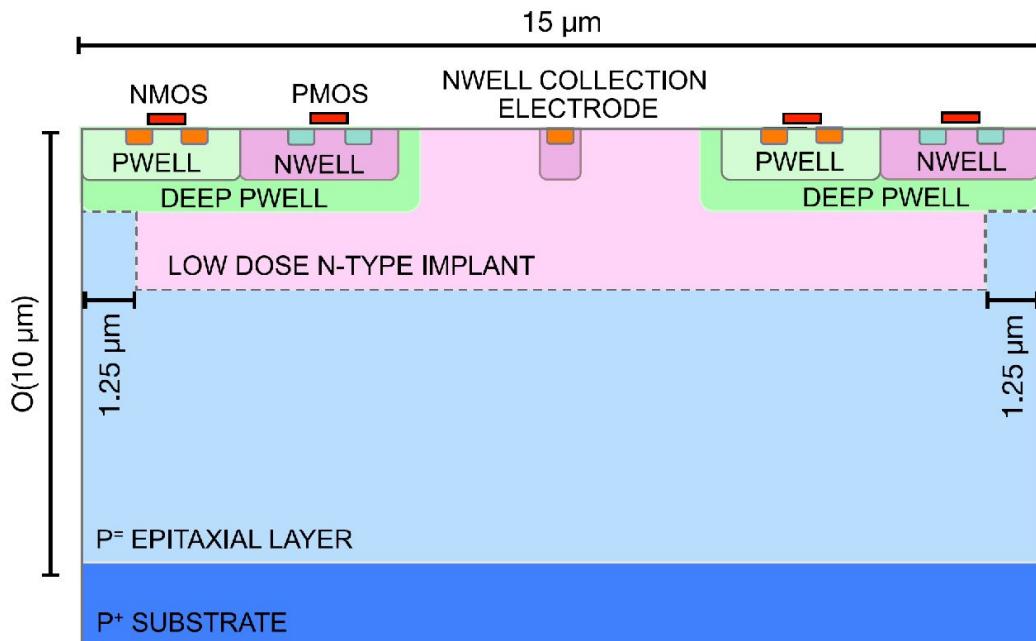
- A serial powering architecture was selected for the SVT outer barrel
- Requires each EIC-LAS to interface with an AncASIC that generates floating power supplies and handles all communications



- DC coupled CML-like TX-RX link used between AncASICs
- Each IpGBT E-Link shares 3 signals: SC_In, SC_Out, CL_In

Need for negative voltage generation

- Required to bias the substrate of the EIC MAPS.
- Prototype has been developed at CERN for the ALICE ITS3 upgrade and demonstrated as the digital pixel test structure (DPTS).



Need for negative voltage generation (2)

- Effect of substrate bias voltage (V_{sub}) is visible in the pixel threshold and noise distributions.
- Values of -1.2V to -3V are sufficient for the DPTS, but even larger values (up to -6V) may be useful for later versions of the sensor.
- Negative voltage can be used to bias other chips within the ePIC detector, such as AstroPix.

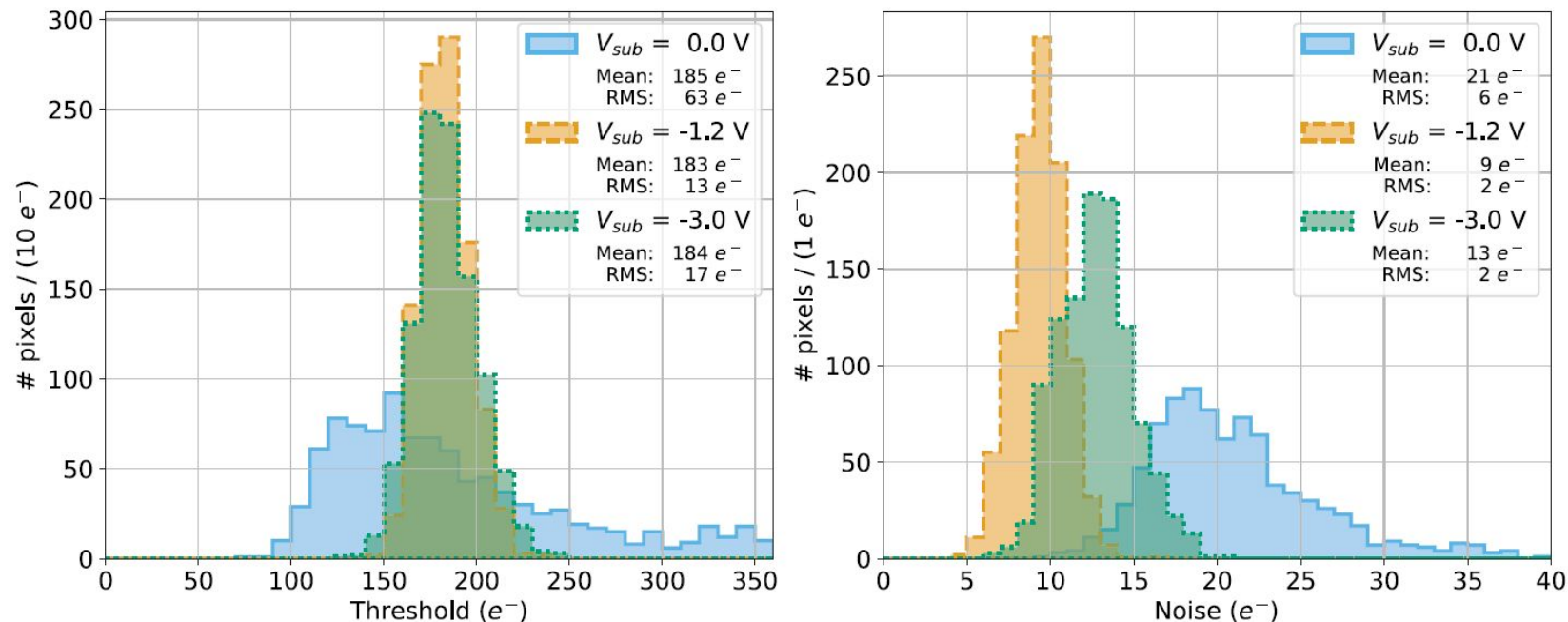


Fig. 7. Pixel threshold (left) and noise (right) distributions of a chip tuned to a threshold of $180 e^-$ with $V_{casb} = 110, 180$ and 500 mV at $V_{sub} = 0.0, -1.2$ and -3 V, respectively. Other chip bias settings are at nominal values (cf. Section 3.1).

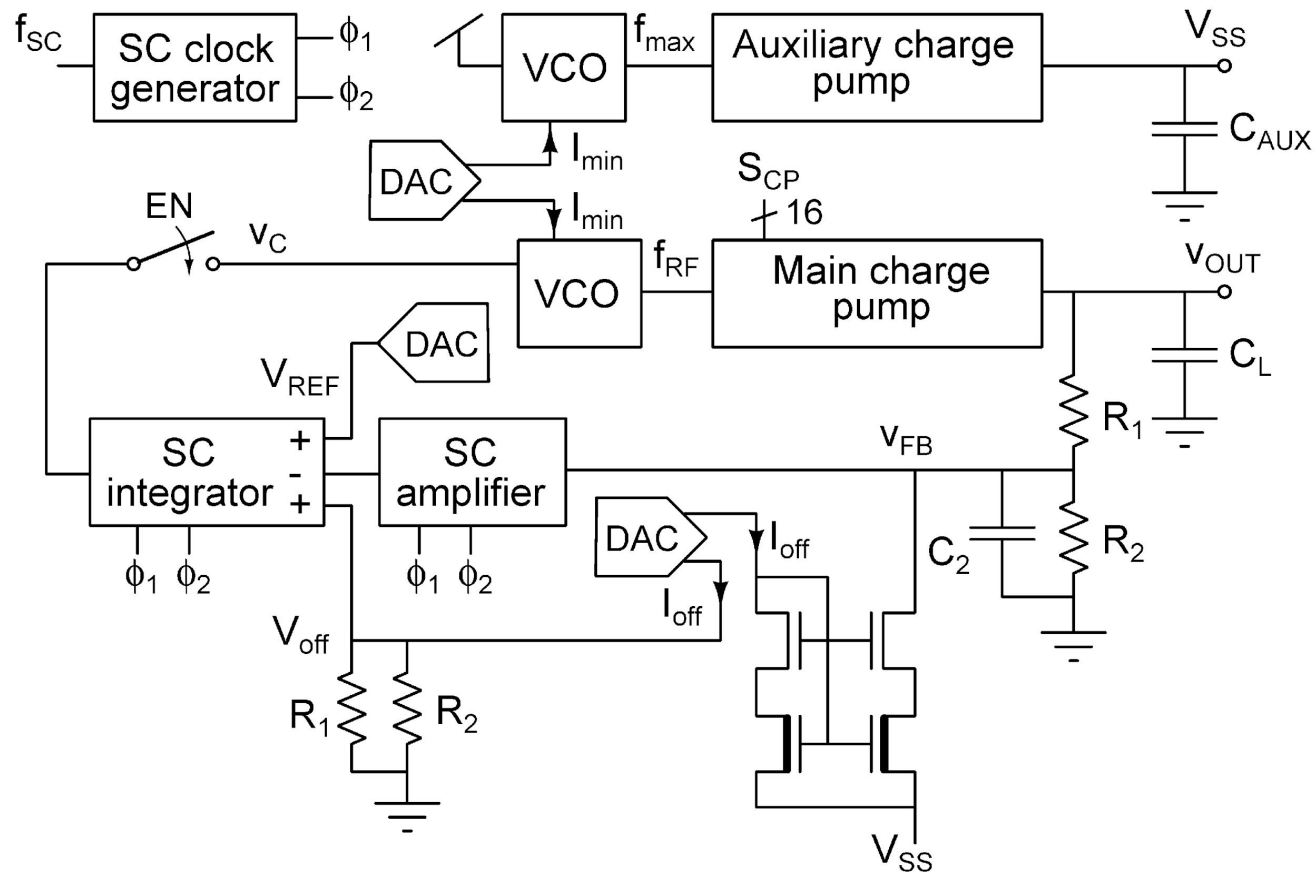
Design specifications

- All circuits should run off a single power supply input ($=1.2\text{ V}$).
- The expected load current is $\sim 200\text{ }\mu\text{A}$, but the negative voltage regulator should support currents up to $\sim 1\text{ mA}$ for safety.
- **Chosen process:** X-Fab XT011, which is a PDSOI process with deep trench isolation (DTI) between individual substrate blocks.
- The availability of DTI is critical for generating voltages that are negative with respect to the substrate. Bulk processes do not allow any p-n junctions to be biased negative with respect to the substrate since this always forward-biases a substrate diode.
- The design only uses thin-oxide (1.5 V) transistors to ensure adequate radiation hardness. This is not a problem for generating large negative voltages as long as individual V_{GS} and V_{DS} values are limited to 1.5 V .

Soumyajit Mandal, Grzegorz W. Deptuch, and Prafull Purohit. “An Integrated Negative Bias Voltage Generator for Stitched Pixel Sensors”, *IEEE Midwest Circuits and Systems Conference (MWSCAS)*, Lansing, MI, August 2025.

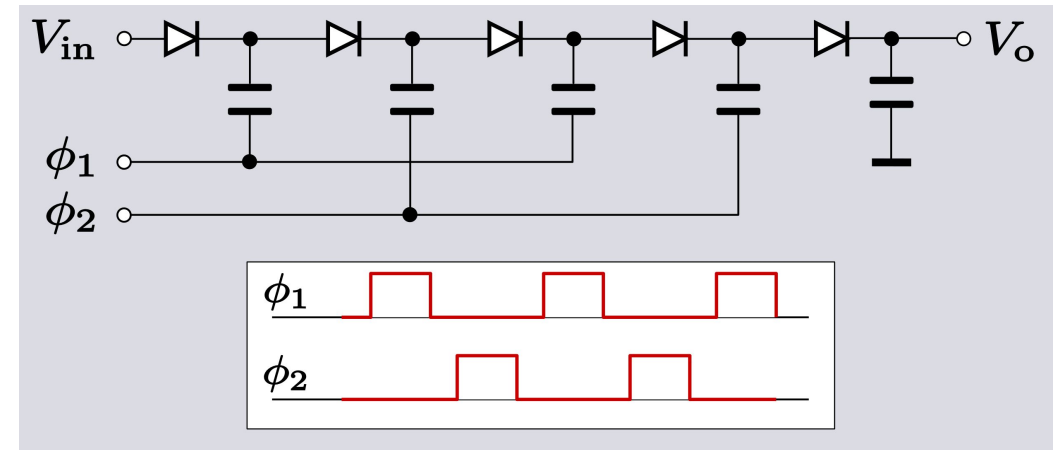
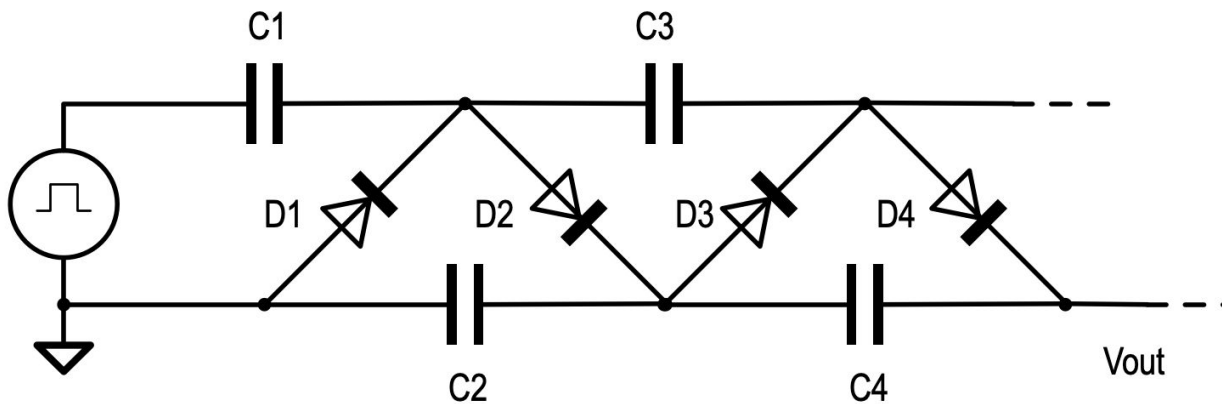
Top-level architecture

- Inverting sensor needed for closed-loop operation of the negative voltage regulator.
 - Converts the negative output voltage to positive form, thus allowing it to be regulated.
- Basic negative regulator circuit consists of
 - A 5-stage Dickson charge pump to generate voltages as low as -6 V.
 - A voltage divider (20:1) to ensure that the negative input voltage does not exist one diode drop ($< 300 \text{ mV}$).
 - A switched-capacitor (SC) amplifier that provides accurate voltage gain (equal to 3 in this case).
 - A current mirror to provide an input voltage offset, which ensures that the output of the SC amplifier stays within its range ($0.2\text{V} - 1\text{V}$).
 - The offset current mirror is biased by a single-stage auxiliary charge pump that generates -1.2V .



Diode-based charge-pump circuits

- Two main topologies: Cockcroft-Walton and Dickson (hybrids are also possible).
- **Cockcroft-Walton**: RF signal is fed in series.
 - The DC voltage across each capacitor is limited to $\sim V_{RF}$, so very high output voltages are possible.
 - The output impedance increases rapidly with number of stages since all the capacitors are in series.
- **Dickson**: RF signal is fed in parallel
 - The DC voltage across each capacitor equals V_{OUT} , limiting the maximum output voltage.
 - The output impedance increases less rapidly since the capacitors are in parallel.
- The current design requires a modest output voltage, so the Dickson topology is preferred.



Transistor-based charge pump circuit

Far Field RF Power Extraction Circuits and Systems

by

Soumyajit Mandal

B.Tech Electronics and Electrical Communication Engineering
Indian Institute of Technology, 2002

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2004

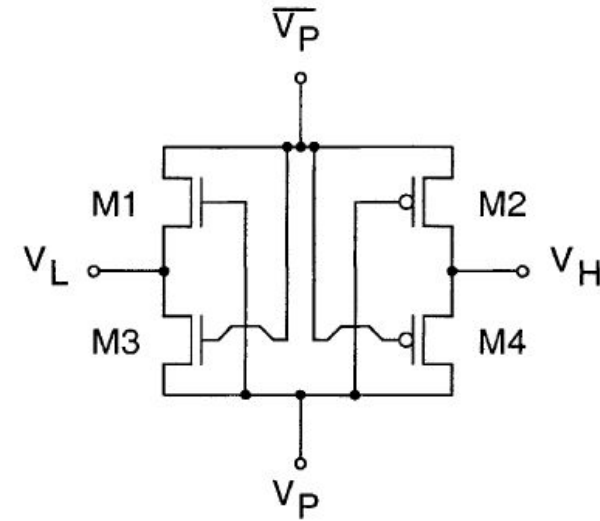


Figure 3-3: The four transistor cell using MOS devices. Body (bulk) terminals are not shown.

- Inverting positive voltages to negative ones requires a switching circuit (AC-DC converter or rectifier).
- The four-transistor cell is an efficient CMOS rectifier.
 - RF input signal is differentially injected between V_P and $\bar{V}_P$.
 - DC output signal builds up between V_L and V_H .
 - Flipping input/output DC terminals allows use either as a positive or negative charge pump.

Transistor-based charge pump circuit (2)

- Typical input and output waveforms show that the no-load DC output voltage is approximately $2V_{RF}$ (i.e., the differential RF drive).
- Multiple four-transistor cells can be connected in series for DC (and in parallel for RF) to generate larger DC output voltages. This topology resembles a Dickson charge pump.

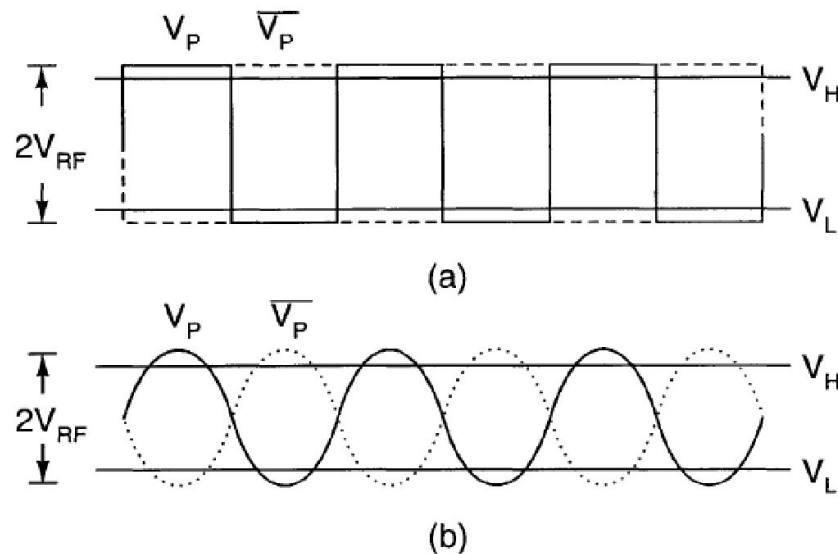


Figure 3-4: Typical steady state waveforms produced by the four transistor switching cell for (a) square wave and (b) sinusoidal inputs.

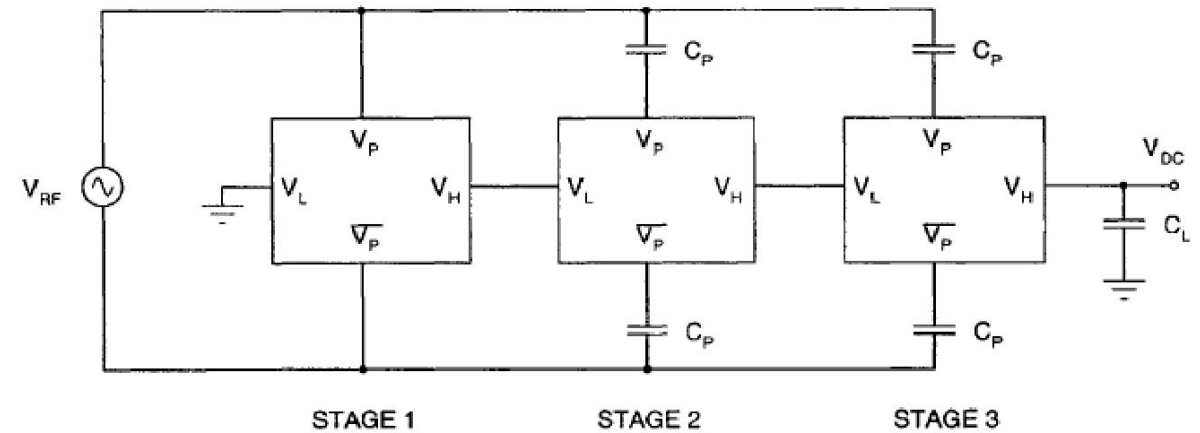
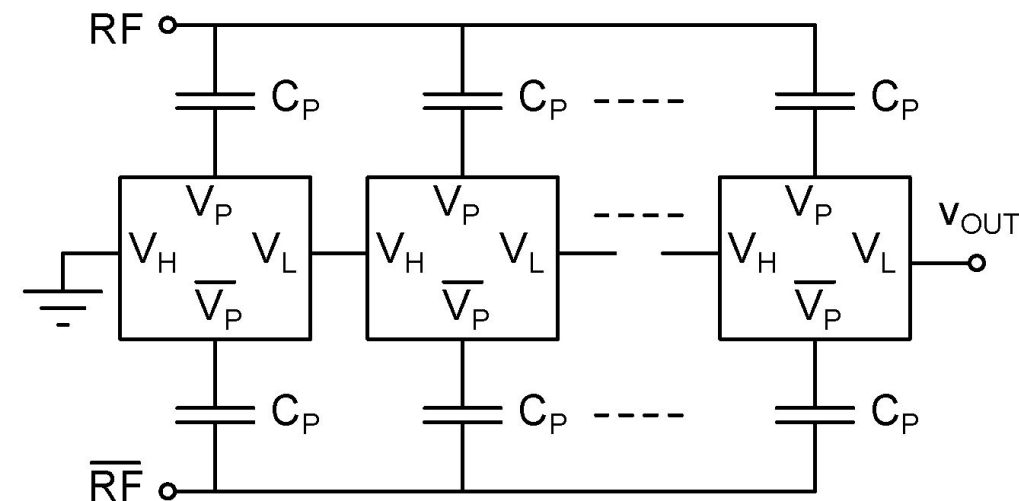
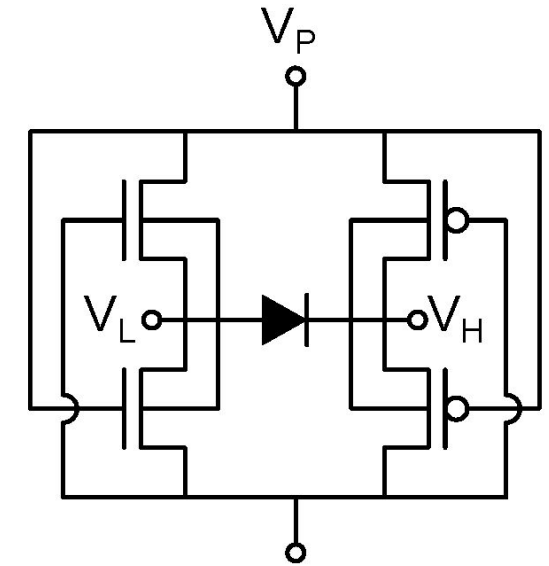


Figure 3-6: A rectifier formed by cascading three switching cells in series. For power extraction applications V_{RF} is generated by an antenna and impedance matching network.

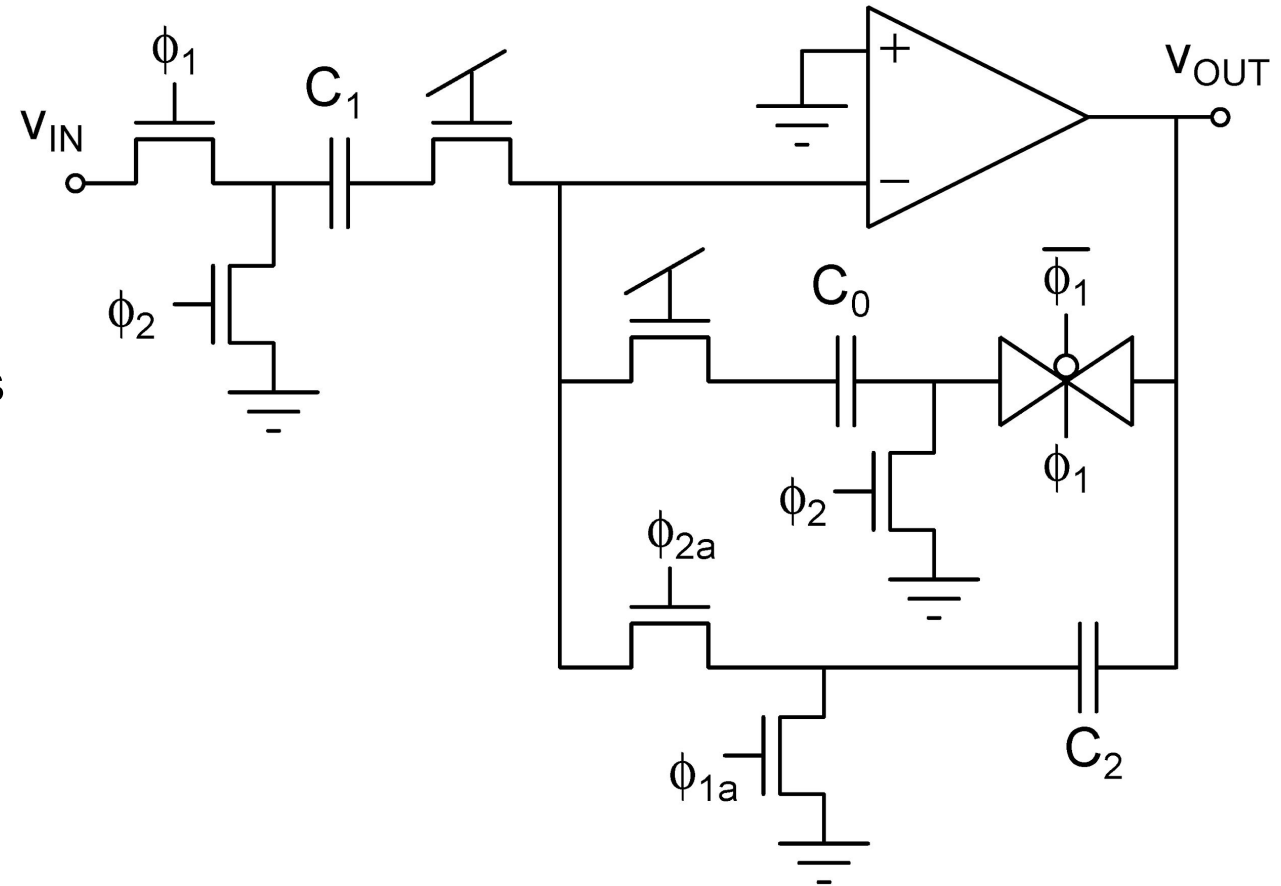
Design of the charge pump

- Use of DTI allows the negative output voltage (V_L) to go below the substrate potential (assumed to be ground).
- Device widths are set to ensure low-enough on resistance for the maximum anticipated load current of 1 mA.
- Auxiliary diode between V_L and V_H acts as a passive rectifier that ensures initial start-up.
- The value of C_P , the pump capacitor, can be programmed to adjust the output impedance



Switched-capacitor (SC) amplifier

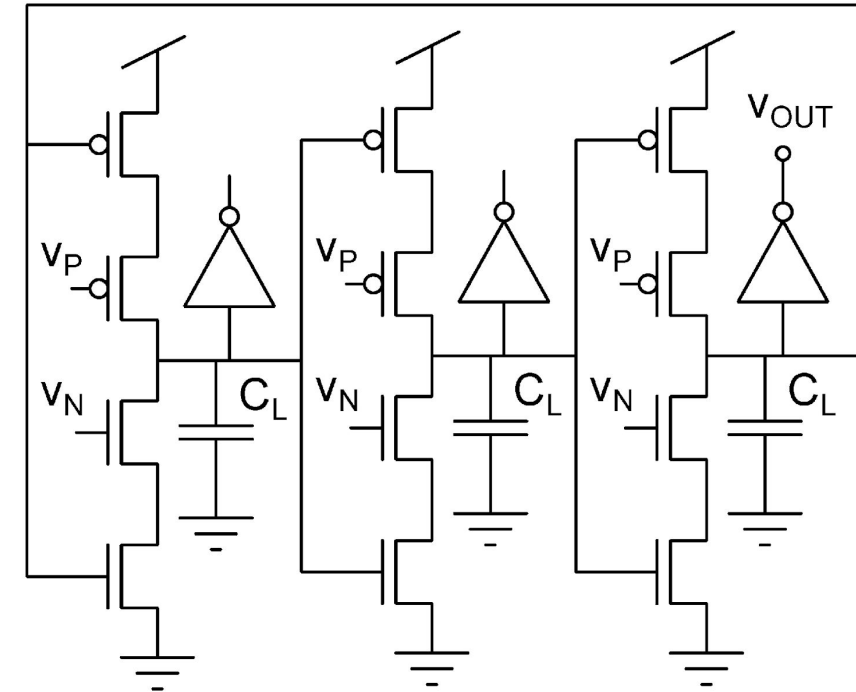
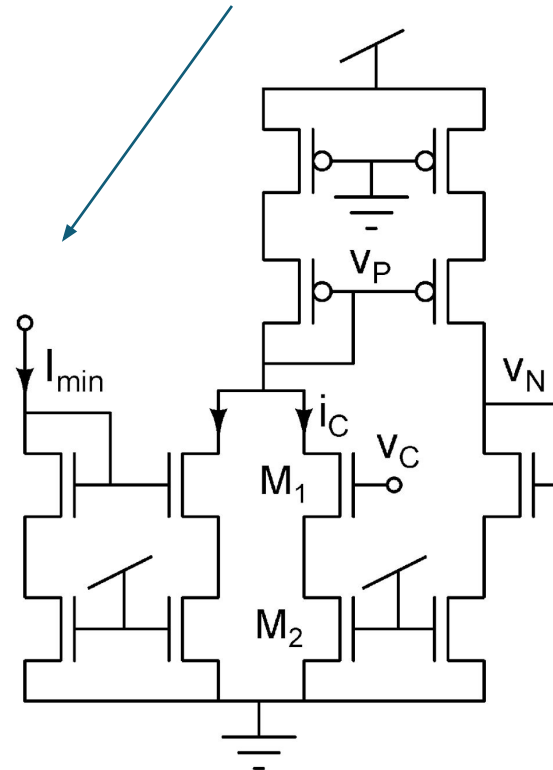
- Classic single-ended SC amplifier with correlated double sampling (CDS)
- Additional hold capacitor reduces output slew rate requirements
- Voltage gain, $A_v = -C_2/C_1$
- Requires two non-overlapping clock phases
- MOS resistors in series with the capacitors reduces glitching at clock edges



VCO design

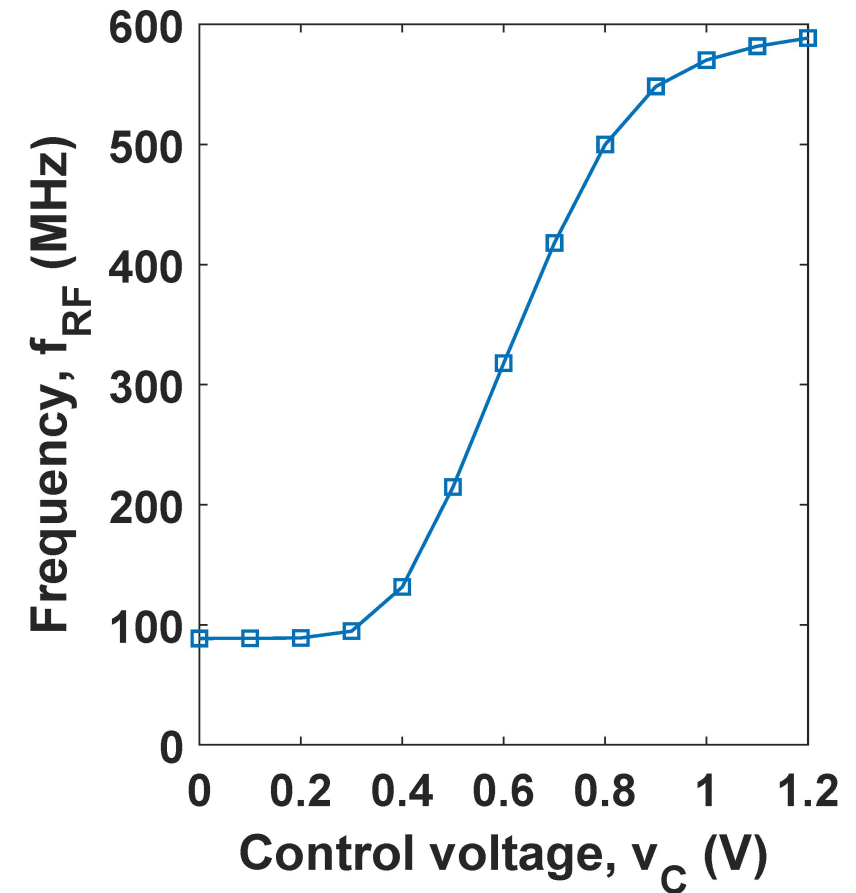
- Simple ring VCO using current-starved inverters to adjust the RF drive frequency
- Control curve is approximately linear in current
 - Minimum frequency is set by $I_{\min}$
 - Maximum frequency is set by the control current at $V_c = V_{DD}$
 - Allows the oscillation frequency range to be adjusted to ensure a monotonic response

Minimum VCO current



VCO simulation

- Range of control currents corresponds approximately to the entire range of V_c (0 to 1.2V)
- Oscillation frequency range for $I_{\min} = 10 \mu\text{A}$ is ~100 MHz to 600 MHz, which is adequate

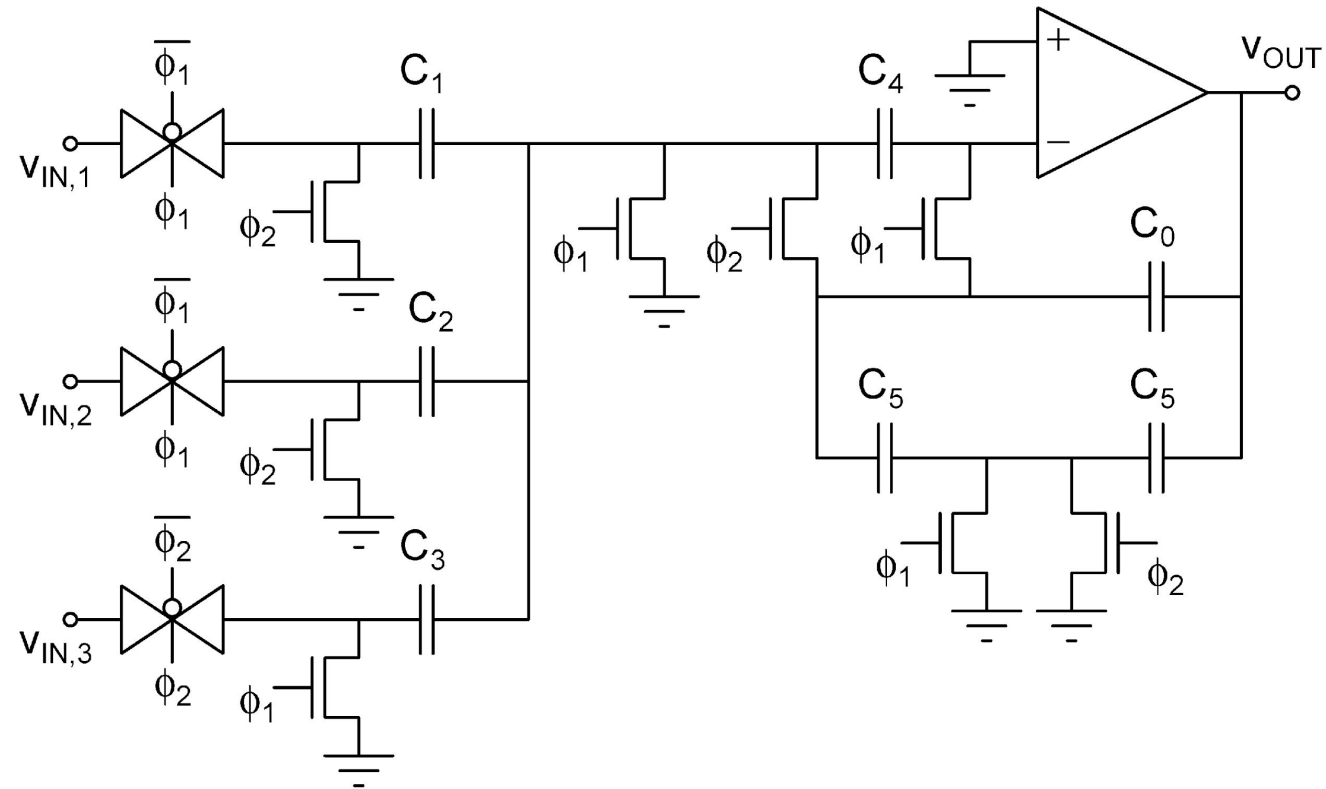


Closed-loop regulator design

- The first step is to pick a suitable **control mechanism**. The main options are:
 - RF drive amplitude, V_{RF}
 - RF frequency, f_{RF}
 - Load current, I_L
 - RF duty cycle, D
- An earlier design (in the XH018 process) used the **RF drive amplitude** as its control mechanism.
 - This works, but results in a highly nonlinear control loop since R_{on} of the charge pump switches changes very rapidly as V_{RF} approaches V_T .
- **Load current control** also works, but results in a highly nonlinear control loop since R_{on} of the charge pump switches is a nonlinear function of I_L .
- **Duty cycle control** is attractive since both R_{on} and Z_p are proportional to $(1 - D)$ for $0 < D < 1/2$, thus resulting in a linear control function.
 - However, it also requires the design of a linear duty-cycle modulator (DCM), which is not trivial.
- **RF frequency control** relies on the fact that the impedance of the pump capacitors is $Z_p = 1/(j\omega C_p)$.
 - Results in a non-monotonic control function due to increased losses at high frequencies due to rise/fall times and device/layout parasitics. Maximum efficiency occurs in the 500-600 MHz range.
 - Circuit implementation is straightforward; chosen for this design.

Switched-capacitor integrator

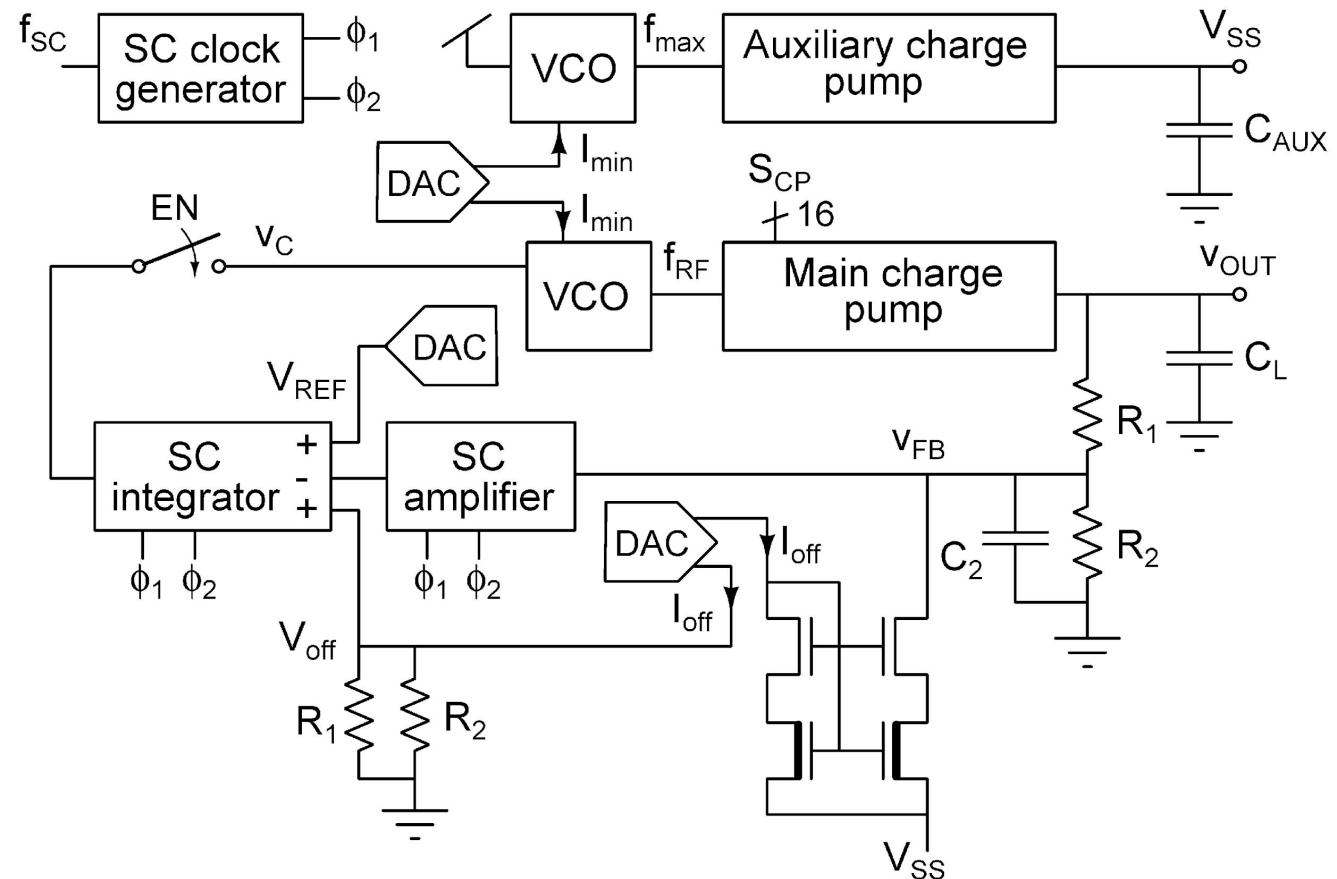
- Final element required to close the feedback loop
- Standard parasitic-insensitive switched-capacitor integrator circuit
- Multiple inputs supported via summation at the virtual ground node
- Sign of the inputs can be individually set via the phase of the input sampling switch
- This design requires three inputs:
 - Input 1 (+): Reference voltage input (from external DAC)
 - Input 2 (+): Offset cancellation voltage ($V_{OFF} = I_{OFF} R_{FB}$ where I_{OFF} is a copy of the current used to create the original offset)
 - Input 3 (-): Feedback voltage from the switched-capacitor amplifier



$$v_{OUT}(z) = \frac{C_1}{C} \left(\frac{1}{z-1} \right) v_{IN,1}(z) + \frac{C_2}{C} \left(\frac{1}{z-1} \right) v_{IN,2}(z) - \frac{C_3}{C} \left(\frac{z^{1/2}}{z-1} \right) v_{IN,3}(z)$$

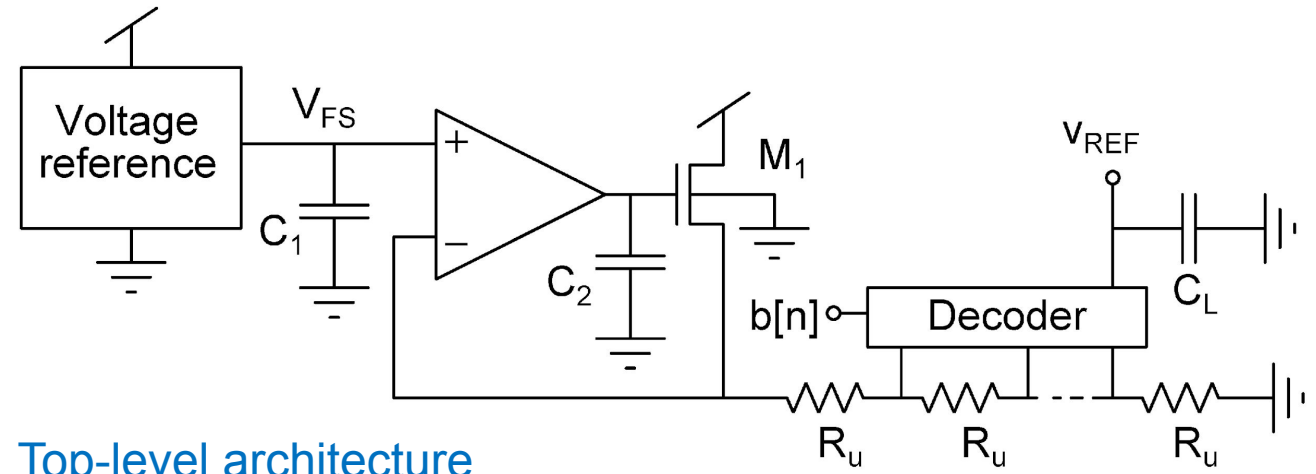
Closed-loop regulator with FM

- Integrator used in the feedback path to set the control voltage, V_C , of the VCO
- Frequency of the auxiliary charge pump is kept fixed at 500 MHz since its output voltage does not need to be adjusted
- RF driver and pump capacitors are split into 16 identical branches
 - Provides coarse control over the output voltage, thus reducing the required control range of the feedback loop
 - Four-bit control variable, S_{CP}
 - Thermometer coding of S_{CP} also provides robustness to single-event upsets
- Nominal values:
 - RF frequency = 500 MHz
 - SC clock frequency = 1 MHz

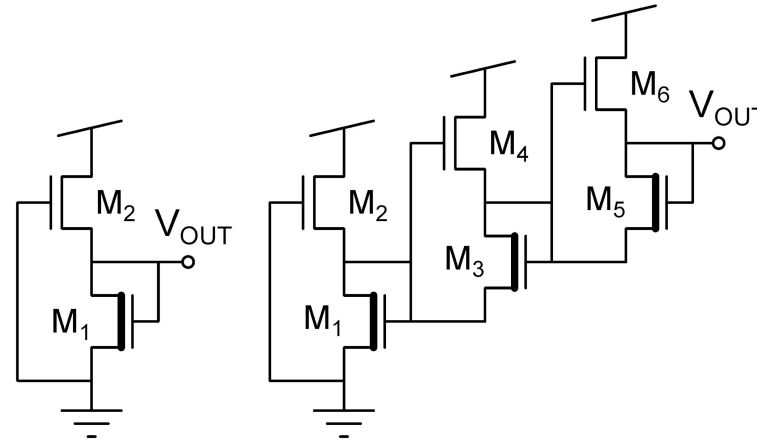


Reference DAC design

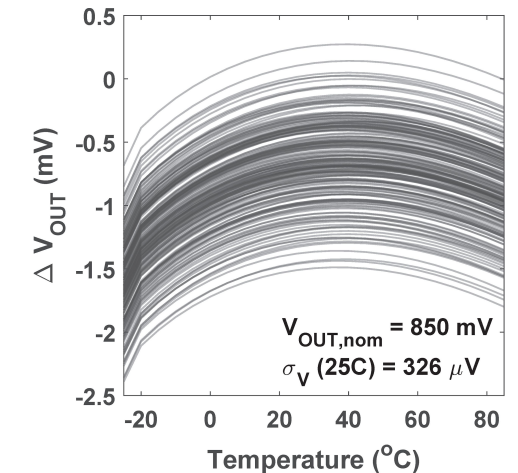
- 8-bit resistor string (Kelvin) DAC driven by a buffered voltage reference ($V_{FS} \approx 850 \text{ mV}$)
- Can operate down to $V_{DD} \approx 1.0 \text{ V}$
 - Voltage reference uses ultra-low-power MOSFET-only topology obtained by stacking two-transistor (2T) references
 - Output source follower uses a natural- V_T NMOS to ensure OTA output is saturated
- Output noise is code-dependent
 - Estimated worst-case error budget (including PVT and noise) is $\sim 1.0 \text{ LSB}$



Top-level architecture



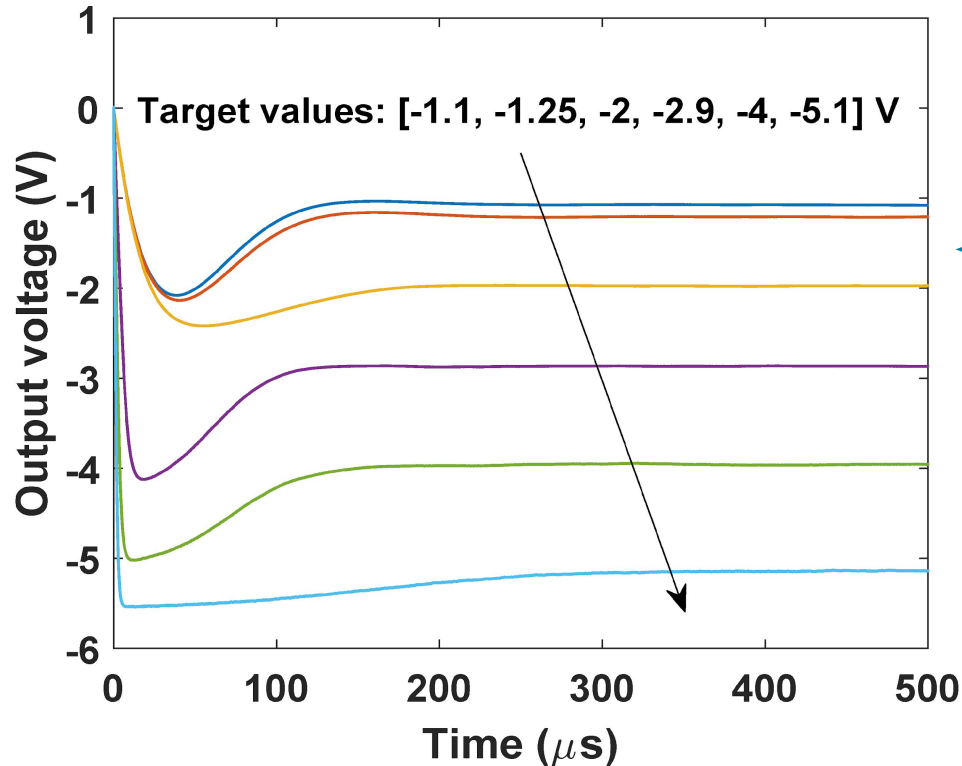
Basic 2T reference (left) and stacked 6T reference (right)



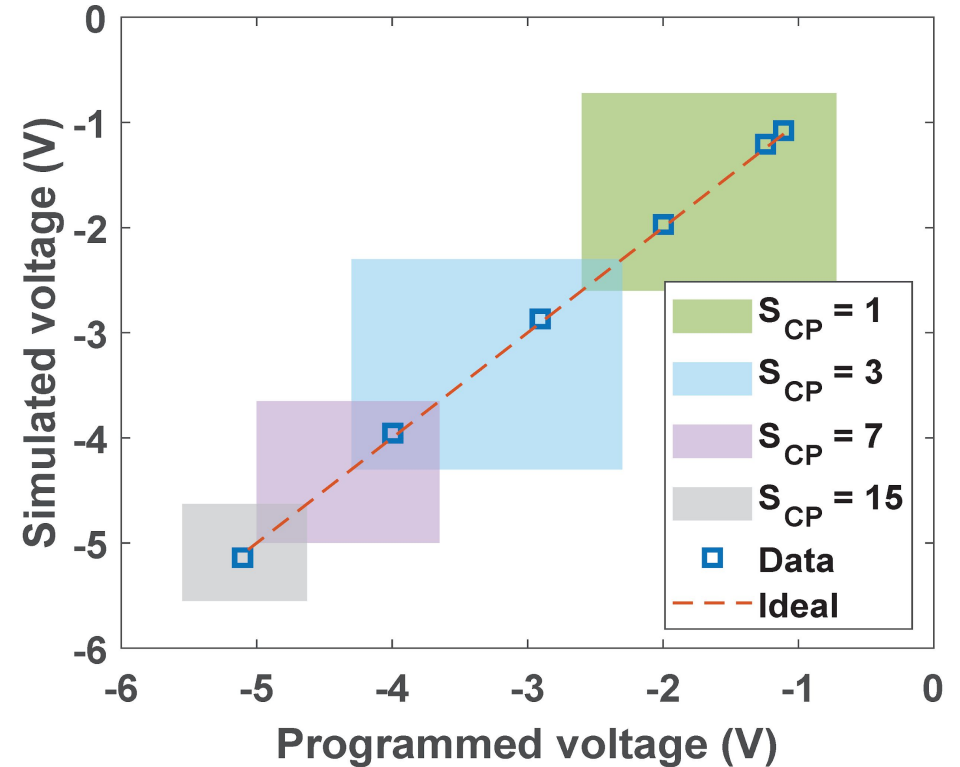
Temperature sweep of 6T reference (Monte Carlo)

Simulations of the closed-loop regulator

- Load current, $I_L = 200 \mu\text{A}$, load capacitance, $C_L = 1 \text{ nF}$



Simulated step responses for various values of D_{REF} and S_{CP} with other parameters kept fixed

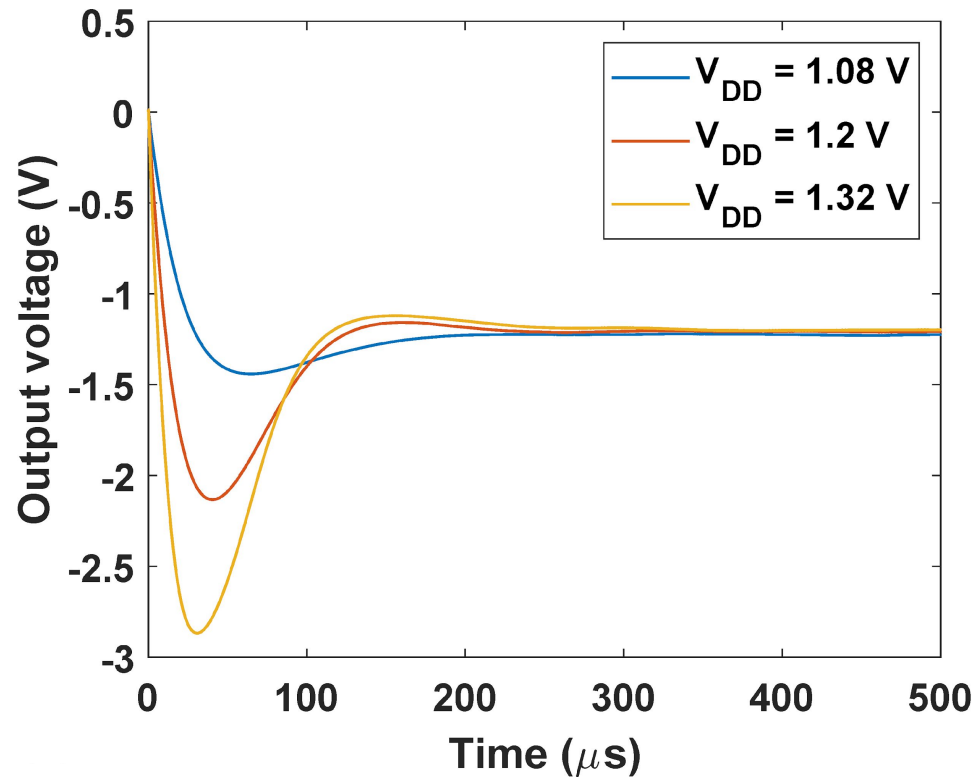


Summary of the steady-state voltages, along with available control ranges for fixed values of S_{CP}

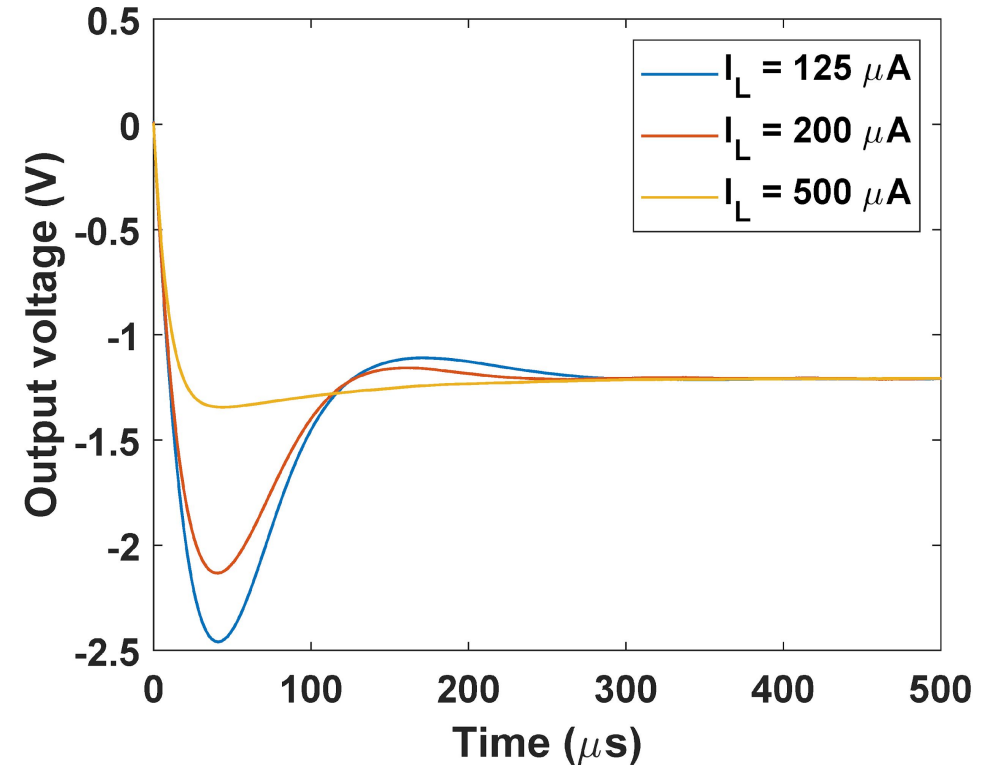
- RF ripple in steady-state varies between $180 \mu\text{V}_{\text{pp}}$ and $640 \mu\text{V}_{\text{pp}}$, which is low enough to ensure negligible ENC degradation of the MAPS analog front-end

Simulations of the closed-loop regulator (2)

- Load current, $I_L = 200 \mu\text{A}$ (nominal), load capacitance, $C_L = 1 \text{ nF}$

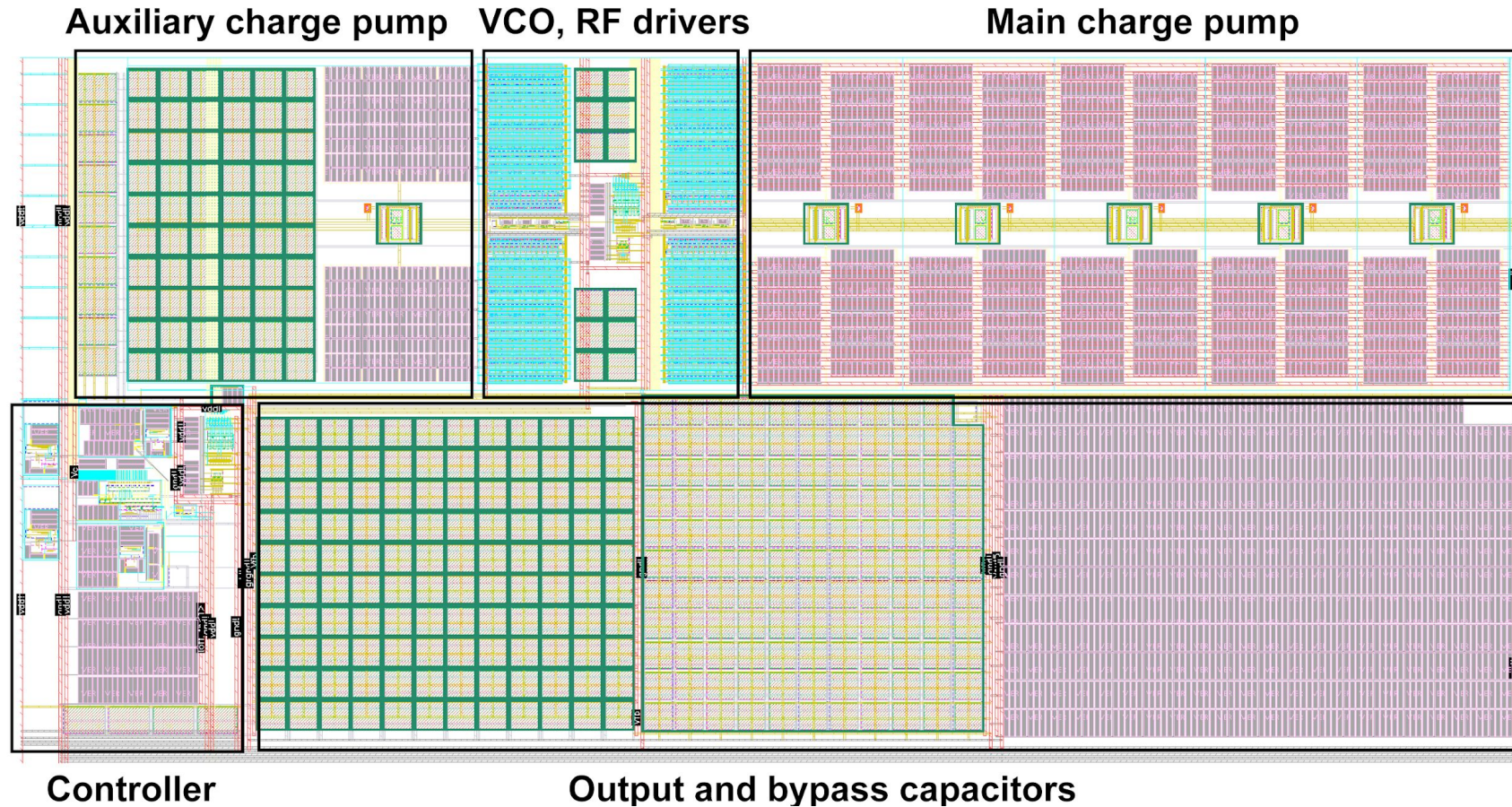


Line regulation: Simulated step responses for $\pm 10\%$ variation in V_{DD} with I_L kept fixed



Load regulation: Simulated step responses for various values of I_L with V_{DD} kept fixed

Complete layout



- Size (not including I²C programming interface) = 1150 μm x 530 μm
- Design is currently being fabricated

Summary

- Presented three projects that require extreme-environment ASIC design (either in terms of temperature or radiation exposure) to meet the needs of high-energy and nuclear physics experiments
- Many of the associated design techniques are also applicable to other harsh environments, such as space
- Requires a highly interdisciplinary set of skills: ASIC designers have to work closely with physicists, mechanical engineers, and data acquisition experts



Backup slides

Subtitle

Backup slides

Subtitle

Shannon-Nyquist Sampling Theorem

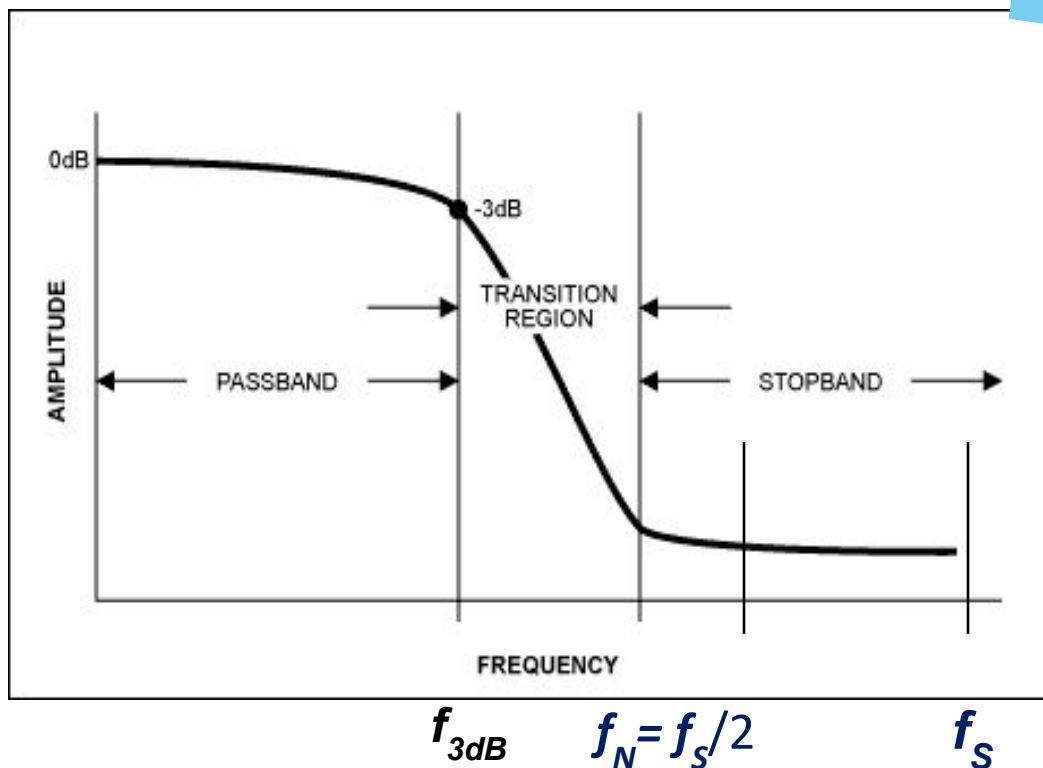
The sampling theorem states that “***unambiguous reconstruction of the signal from its samples is possible when the power of frequencies above the Nyquist frequency, $f_N = f_s/2$, is zero***”,

i.e., the highest frequency component of the sampled signal must be less than half the sampling frequency.

The second rule, which is often forgotten, is that samples must be equally spaced.

Definitions

An anti-aliasing filter is a filter used before a signal sampler (ADC) to restrict the bandwidth of a signal to satisfy the sampling theorem over the band of interest. Since the theorem states that “*unambiguous reconstruction of the signal from its samples is possible when the power of frequencies above the Nyquist frequency, $f_N = f_s/2$, is zero*”; an anti-aliasing filter trades off between the bandwidth and aliasing. A realizable anti-aliasing filter will typically either permit some aliasing to occur or else attenuate some in-band frequencies close to the Nyquist limit. For this reason, many practical systems sample at a higher rate than required to ensure that all frequencies of interest can be reconstructed, a practice called oversampling (adapted from Wiki)



$$M = f_s/2f_N$$

The transition region is determined by the type and order of the anti-aliasing filter.

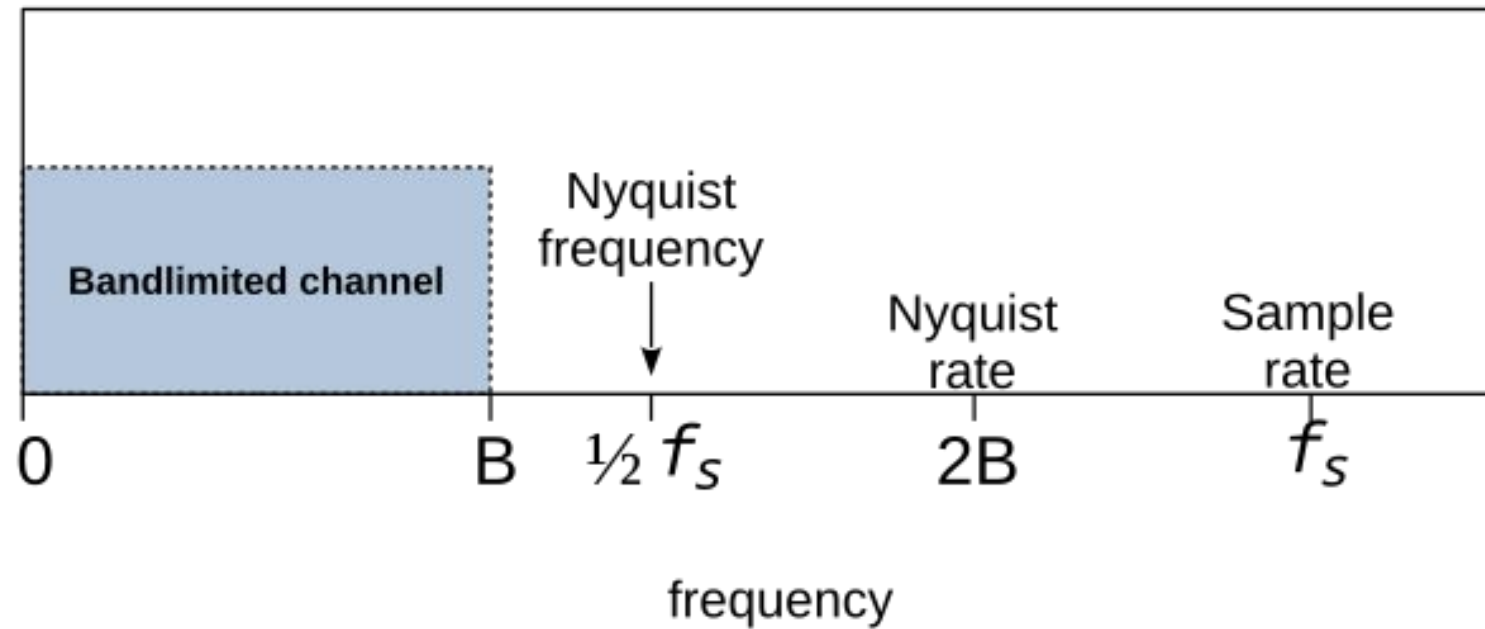
The Nyquist frequency is defined as:

$$f_N = f_s/2$$

Nyquist rate (arbitrary def.):

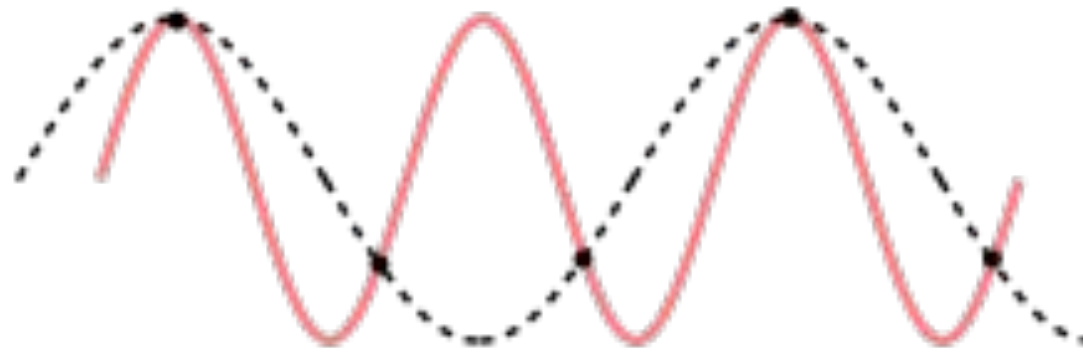
$$f_{NR} = 2 \text{ Bandwidth}$$

Relationship of Nyquist frequency & rate (example)

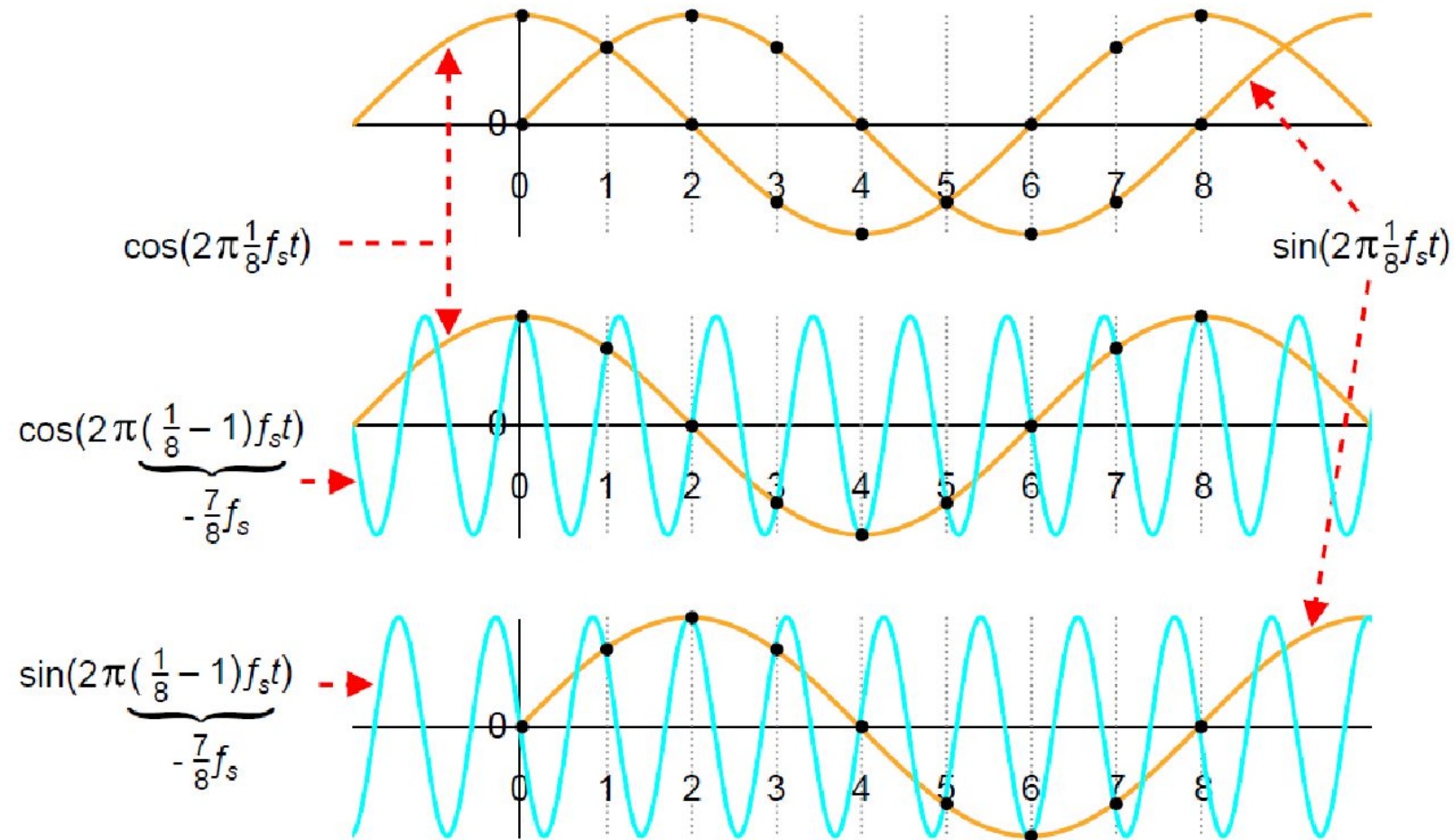


Aliasing (1)

Appearance of frequencies above the Nyquist frequency $f_s/2$ (no anti-aliasing filter)

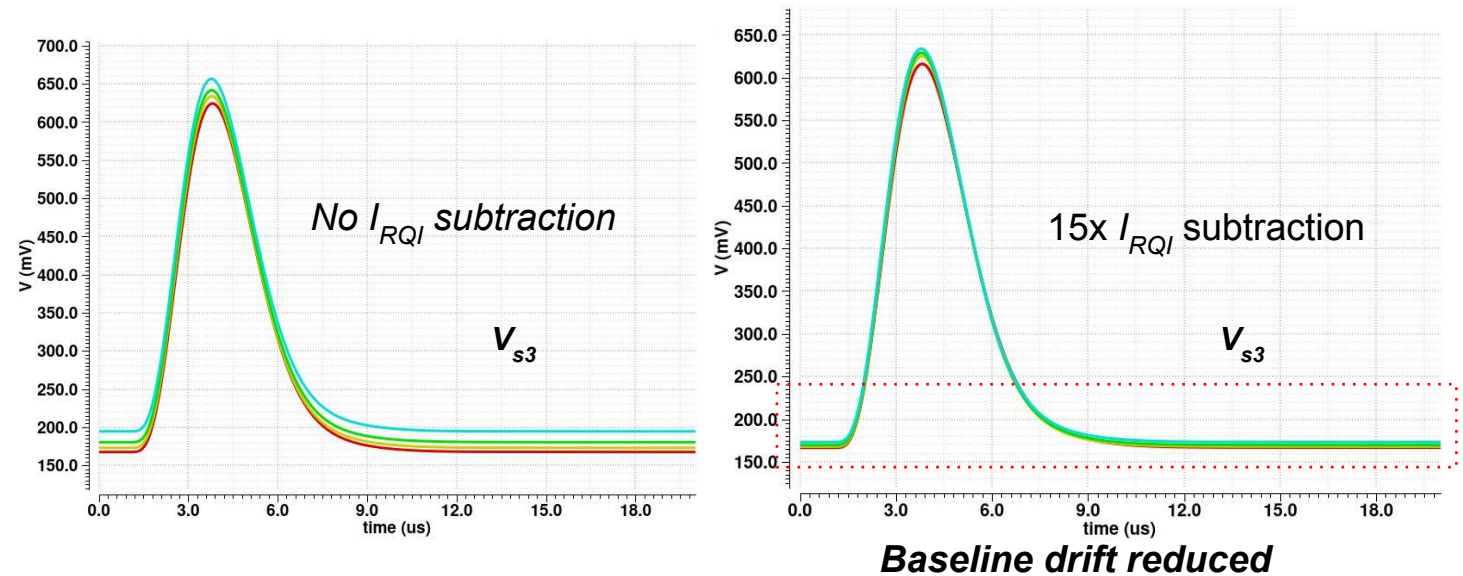
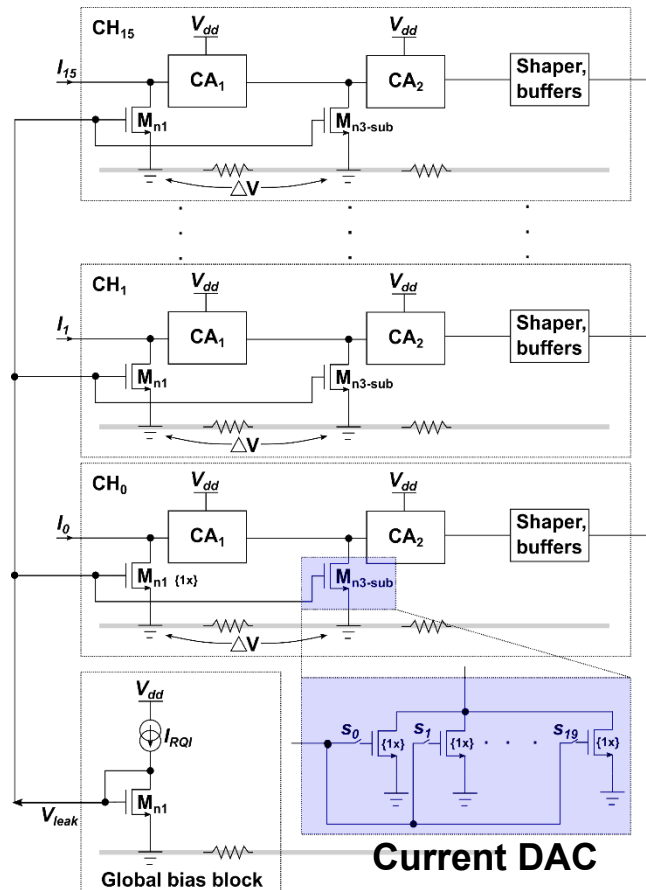


Aliasing (2)



Programmable 5-bit RQI subtraction implemented in CHARMS250

Response with different values of I_{RQI}



- Programmable I_{RQI} subtraction provides immunity against process mismatches and layout induced non-ideality
- For M_{n1} and M_{n3-sub} operating in deep-subthreshold ($I_{RQI} \propto e^{(V_{gs}-V_{th})(q/\eta kT)}$), variance in I_{RQI} at LNT almost 10x higher than at RT
- Previously, with fixed I_{RQI} subtraction, even few-millivolts of V_{gs} difference at M_{n1} and M_{n3-sub} due to IR drop in ground rail was seen to cause subtraction to become > 20x and make the second stage reset mechanism non-operational

Summary

- CHARMS250, a next-generation cryogenic front-end ASIC in 65 nm with 250 ns shortest peaking time currently in development
- Transistor test structures fabricated for performing noise characterization at room and cold temperatures
- Prototype CHARMS250 chip comprising of a single channel to be submitted for fabrication in May 2025
- CHARMS10, a next-generation cryogenic front-end ASIC in 65 nm with 10 ns shortest peaking time also planned to be designed
- Feasibility studies for determining the most suitable front-end amplifier design for CHARMS10 ongoing

Conclusion and future work

- A power-efficient on-chip data link has been designed for large-area stitched pixel sensors
- **Next steps:** Layout a 1.5 x 1.5 mm chiplet containing the proposed solution
 - The transmission line will be designed using a zigzag pattern to save space
 - Chip submission expected in October 2024



Existing design: Current-mode transceiver

- Designed for on-chip global interconnects and silicon interposer channels (tested up to 20 mm).
- Nominal data rate: 3 Gb/s.
- Highly power-efficient: 9.5 fJ/bit/mm (280 μ W for a 10 mm link at 3 Gb/s).
- **Transmitter:** Open drain, one-tap pre-emphasis.
- **Receiver:** Current sense amplifier with active inductor for bandwidth enhancement.

2044

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Current-Mode Transceiver for Silicon Interposer Channel

Seung-Hun Lee, Seon-Kyoo Lee, Byungsub Kim, Hong-June Park, and Jae-Yoon Sim, *Senior Member, IEEE*

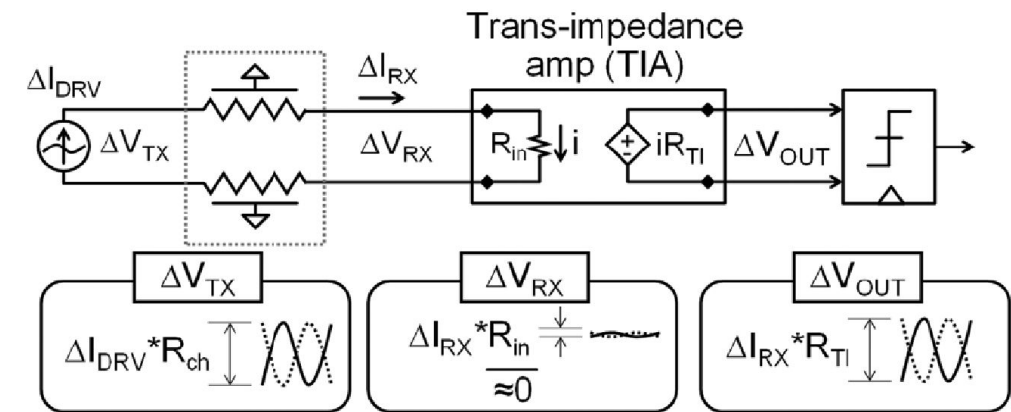
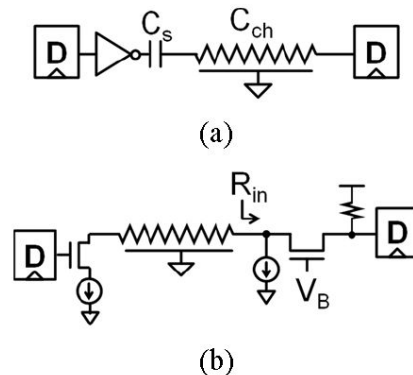
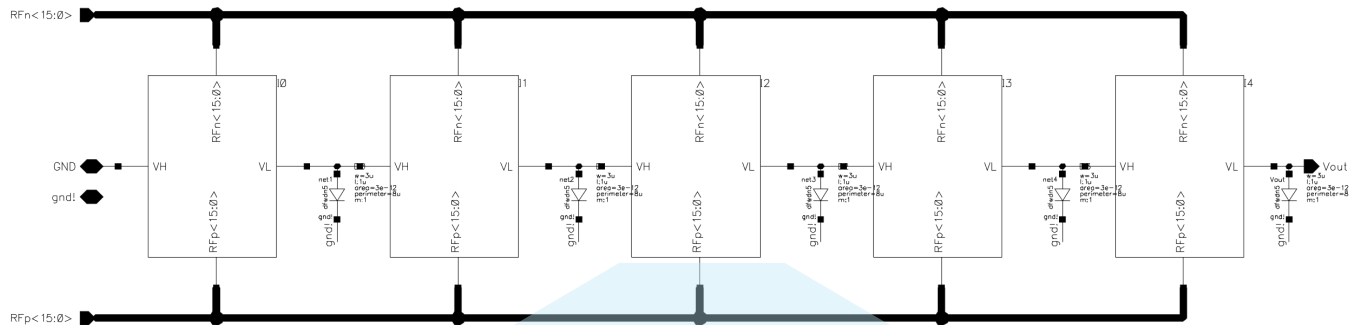


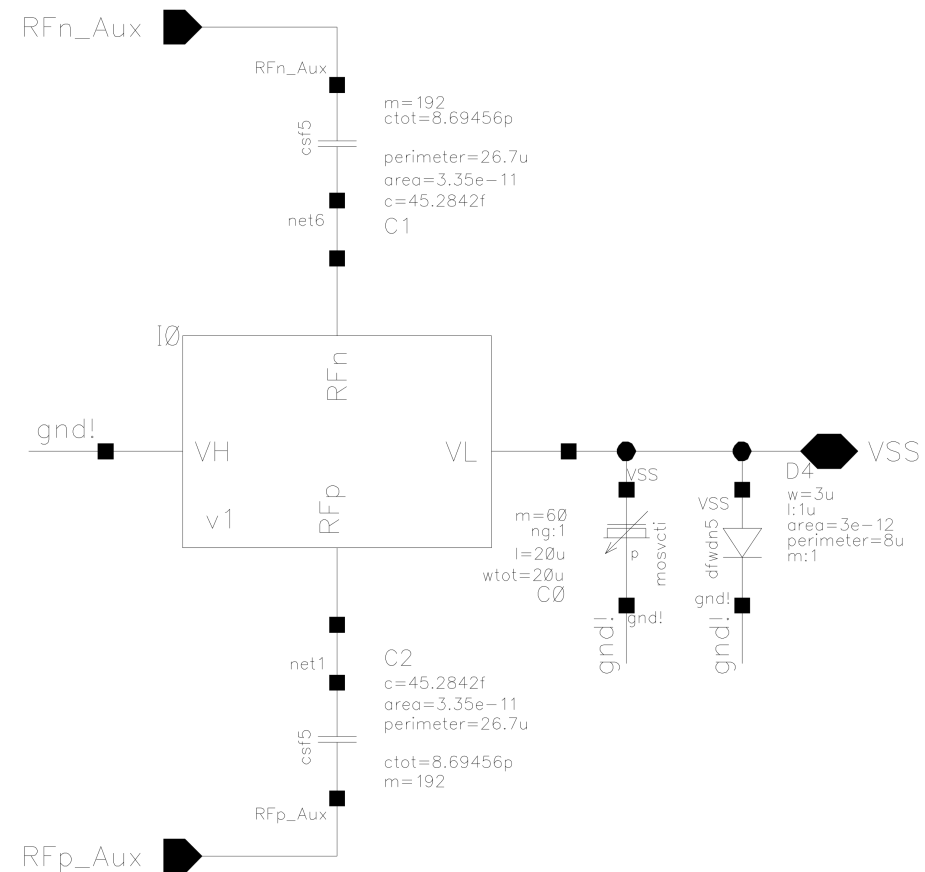
Fig. 2. Concept of the proposed current-mode transceiver.

Charge pump design

Main charge pump



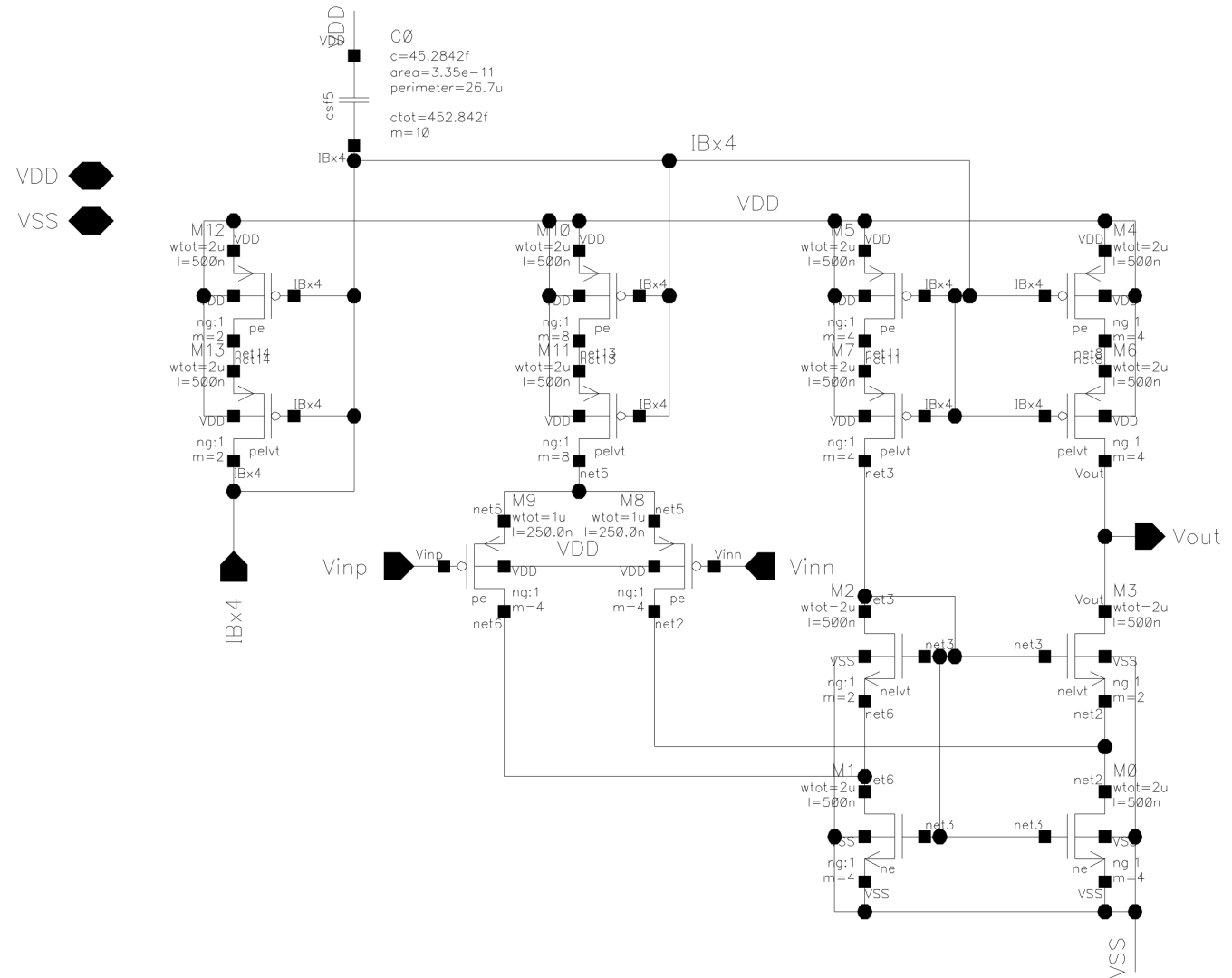
Auxiliary charge pump



Capacitor size programming

OTA design

- Folded cascode with PMOS inputs to ensure operation with $V_{CM} = 0$ V.
- Nominal open-loop gain ≈ 60 dB.



Open-loop simulation results

- RF frequency = 500 MHz
 - Chosen to keep pump capacitor size reasonable
- Load current = 200 μA
- SC frequency = 1 MHz
- Feedback voltage, V_{FB} , is close to the theoretical value
 - V_{OFF} needs to be subtracted out in the feedback path

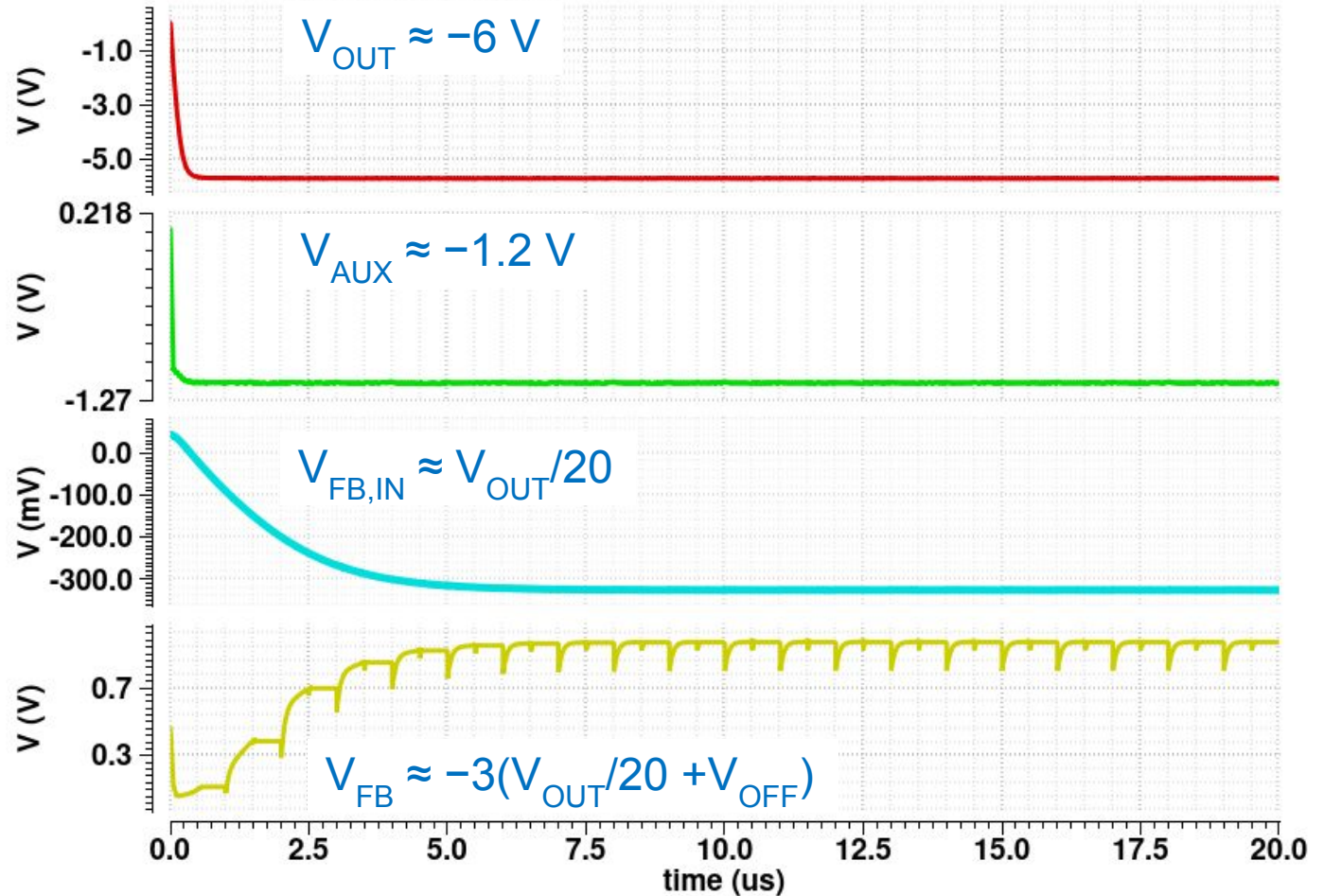
Transient Response
Name

■ /Vout5

■ /VSS

■ VT("/IO/Vfb")

■ /Vfb_g

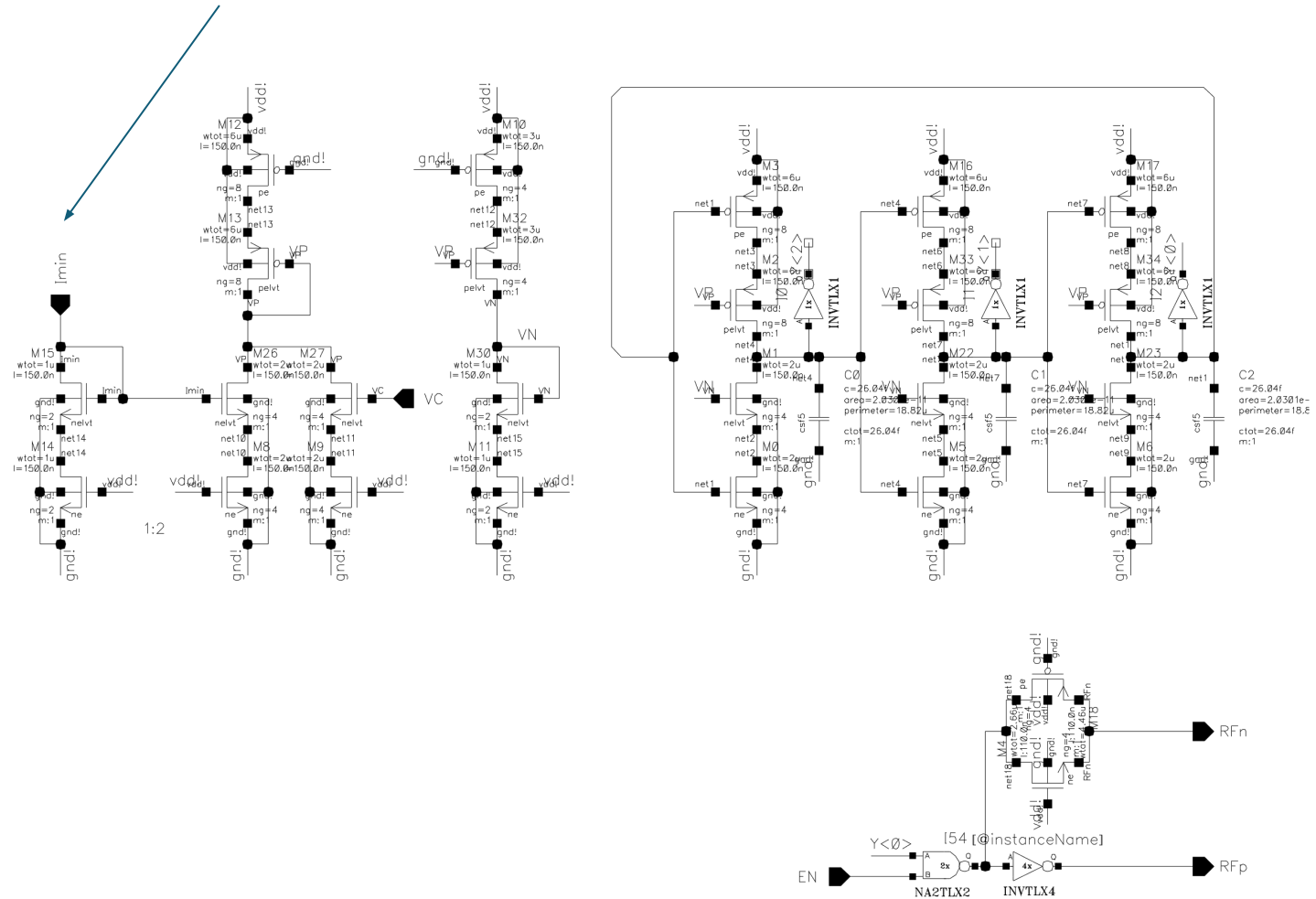


$$V_{\text{OFF}} = I_{\text{OFF}} R_{\text{FB}} \approx 43 \text{ mV}$$

VCO design

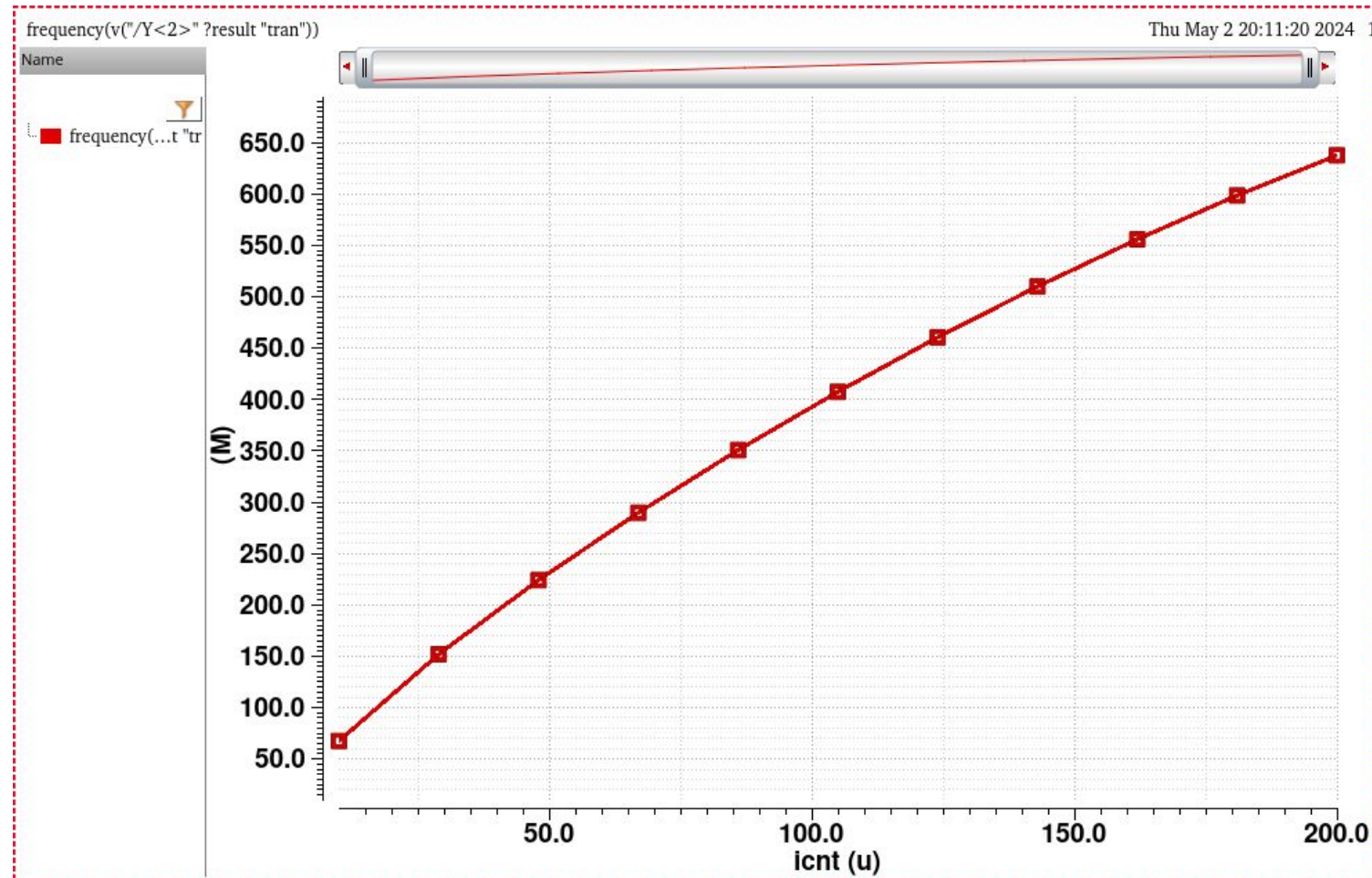
- Simple ring VCO using current-starved inverters to adjust the RF drive frequency
- Control curve is approximately linear in current
 - Minimum frequency is set by $I_{\min}$
 - Maximum frequency is set by the control current at $V_c = V_{DD}$
 - Allows the oscillation frequency range to be adjusted to ensure a monotonic response

Minimum VCO current



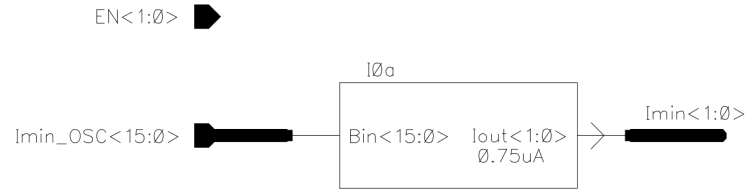
VCO simulation

- Range of control currents corresponds approximately to the entire range of V_c (0 to 1.2V)
- Oscillation frequency range for $I_{\min} = 10 \mu\text{A}$ is $\sim 80 \text{ MHz}$ to 650 MHz , which is adequate

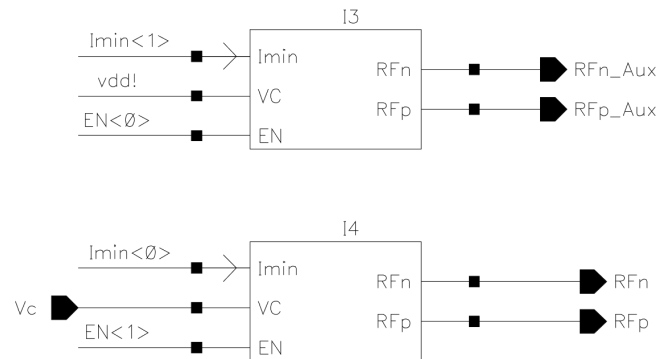


RF driver for charge pumps

Fixed oscillator
for auxiliary
charge pump

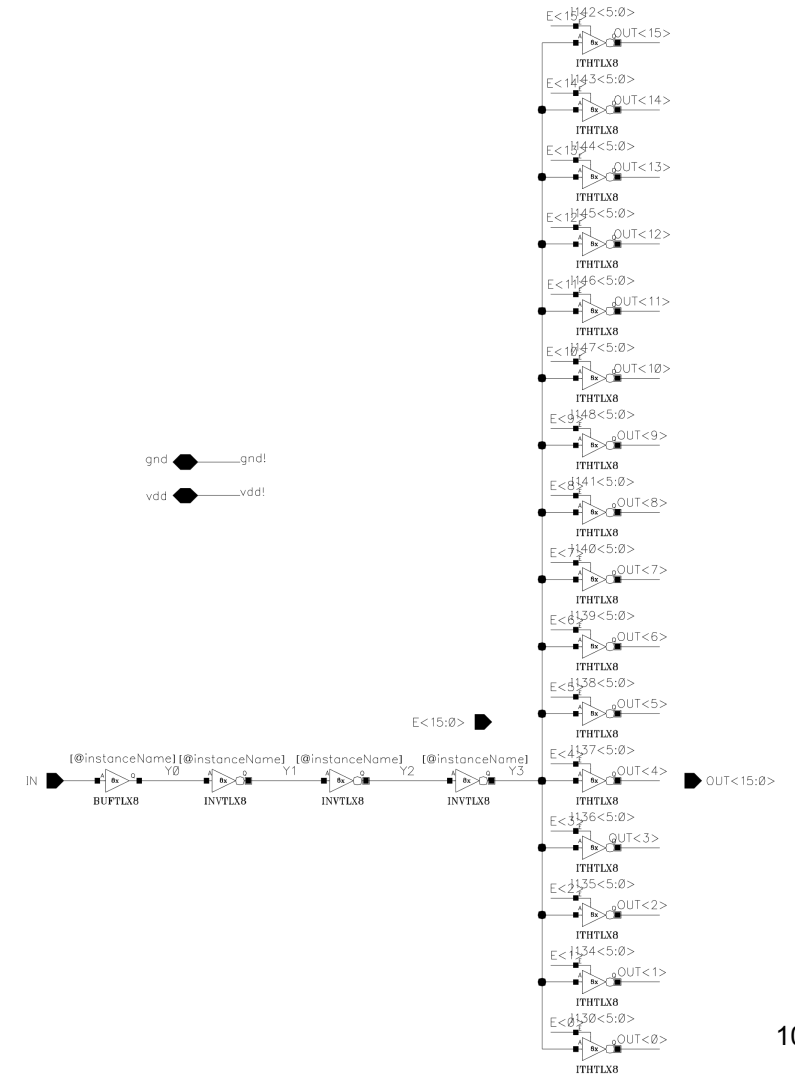


Minimum
current DAC



VCO for main
charge pump

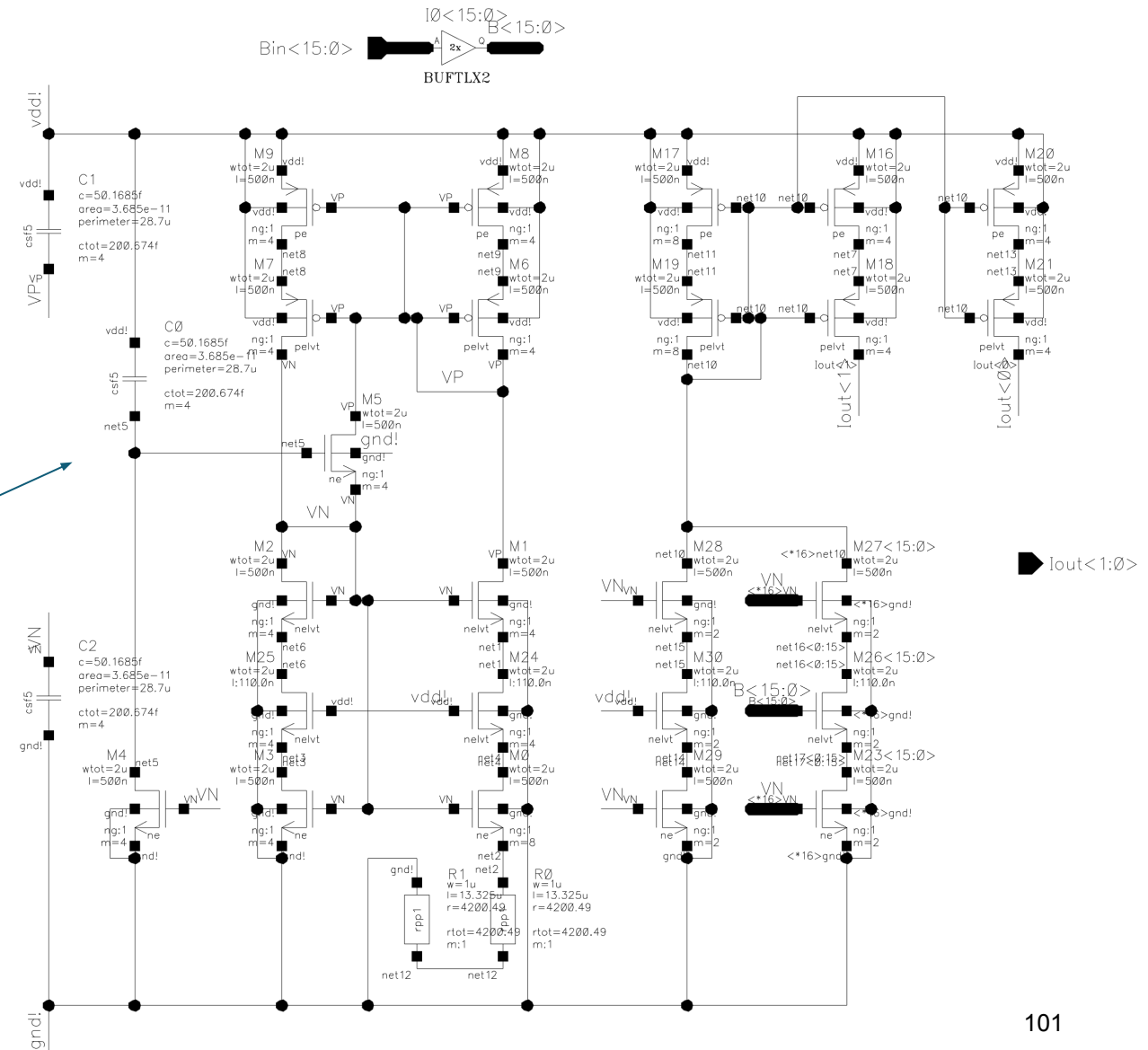
Output buffer



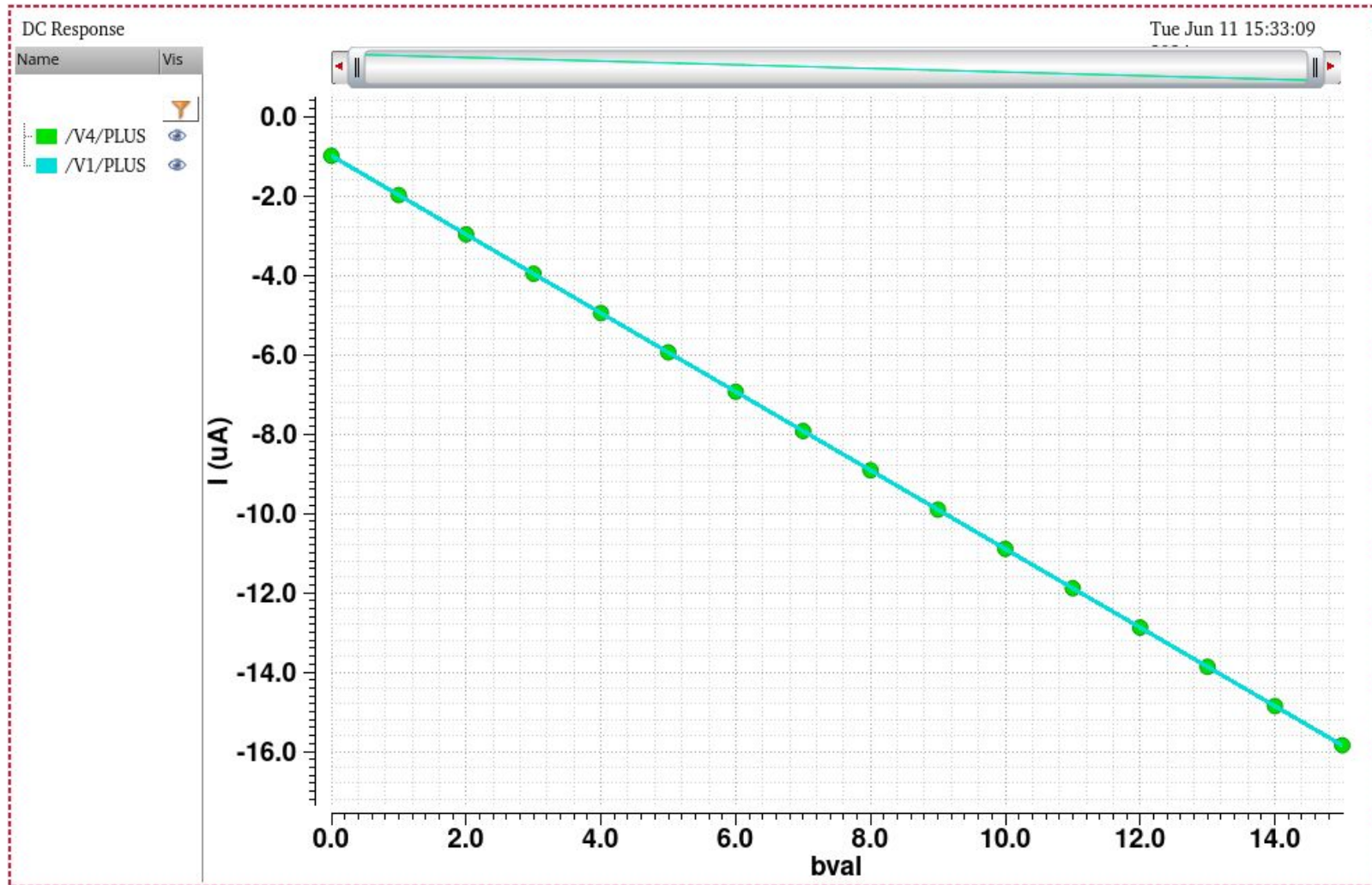
Current DAC

- Constant- g_m reference with 4-bit output current DAC
- Thermometer-coded control signals for improved radiation tolerance
- Similar design used to set all bias currents within the regulator

Startup circuit



Current DAC simulation

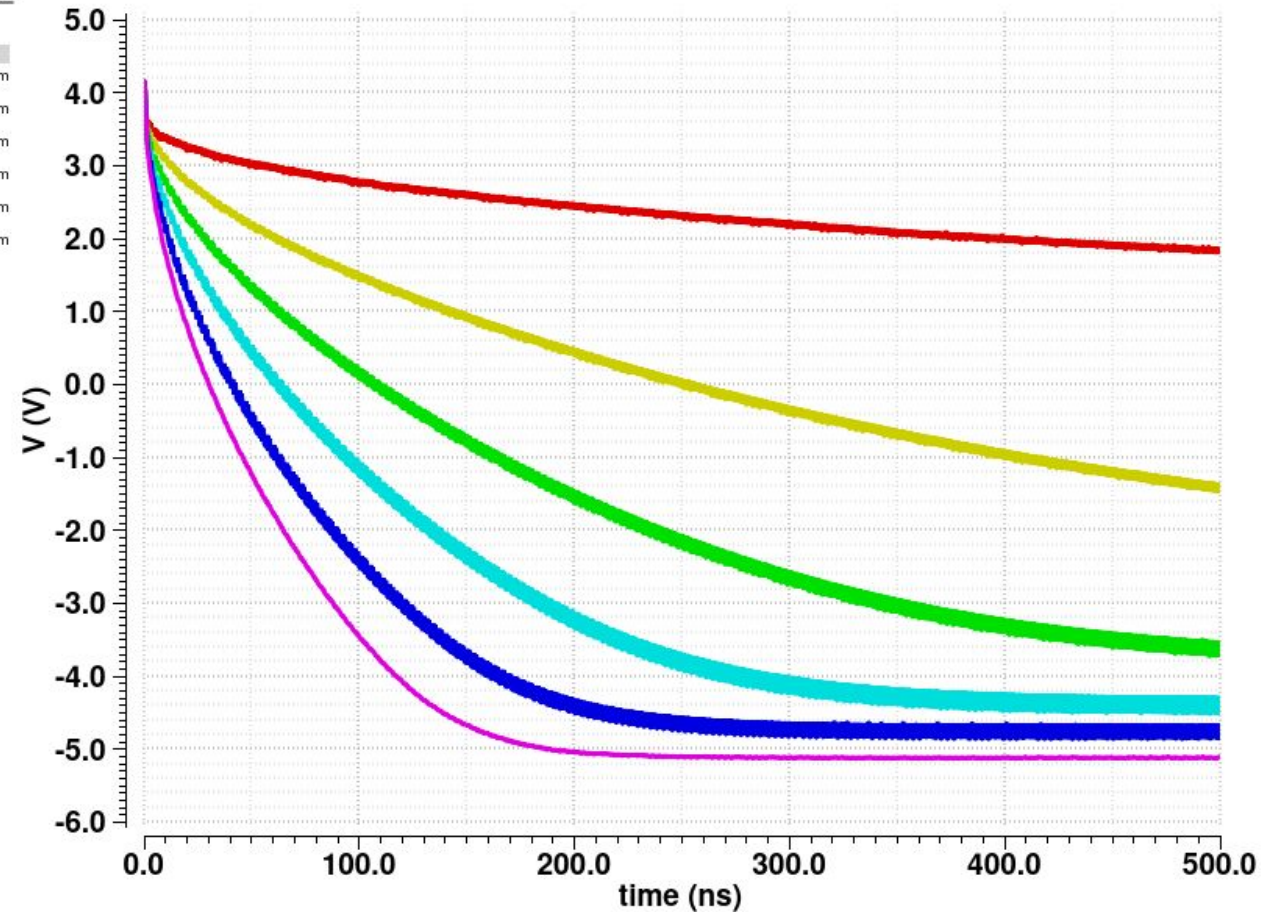


Step size = 1 μ A

Feasibility of duty-cycle control

- Open-loop charge-pump output, V_{OUT} , as a function of D
 - RF frequency = 500 MHz
 - Load current = 1 mA
- Control range of $0.1 < D < 0.5$ is sufficient in this case
 - However, smaller duty cycles will be required for smaller load currents
 - Problems with generating very short pulses can be avoided by only using D for fine control
 - Coarse control can be obtained by using a switched array to vary the pump capacitance, C_P

Transient Response		
Name	...	dcyc
/Vout5		
/Vout5		100.0m
/Vout5		138.0m
/Vout5		190.4m
/Vout5		262.7m
/Vout5		362.4m
/Vout5		500.0m



Duty-cycle modulator (DCM) design

- Based on the DCM design in [1].
- Uses matched VCDLs to generate the difference between a fixed (minimum) and variable time delay.
- Additional logic ensures that the maximum duty cycle is limited to 50%.
- The initial implementation worked but suffered from unwanted latching in the VCDL delay cells and relatively long propagation delays in the standard-cell DFFs.
 - Design was tweaked to improve performance. For instance, the standard-cell DFFs were replaced with custom TSPC DFFs, which are much faster.

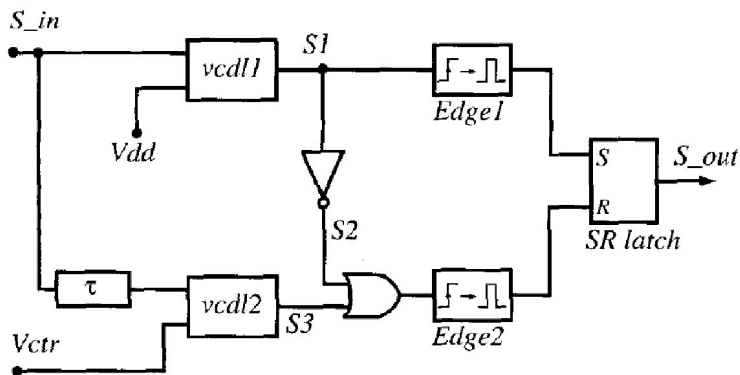
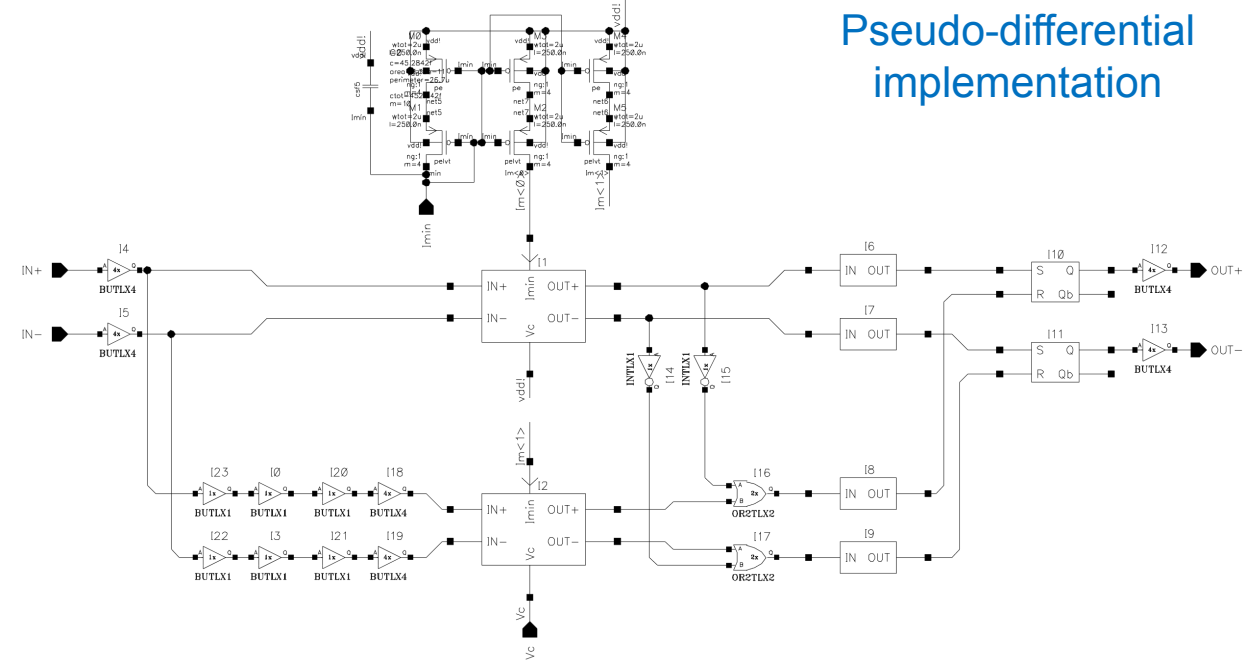
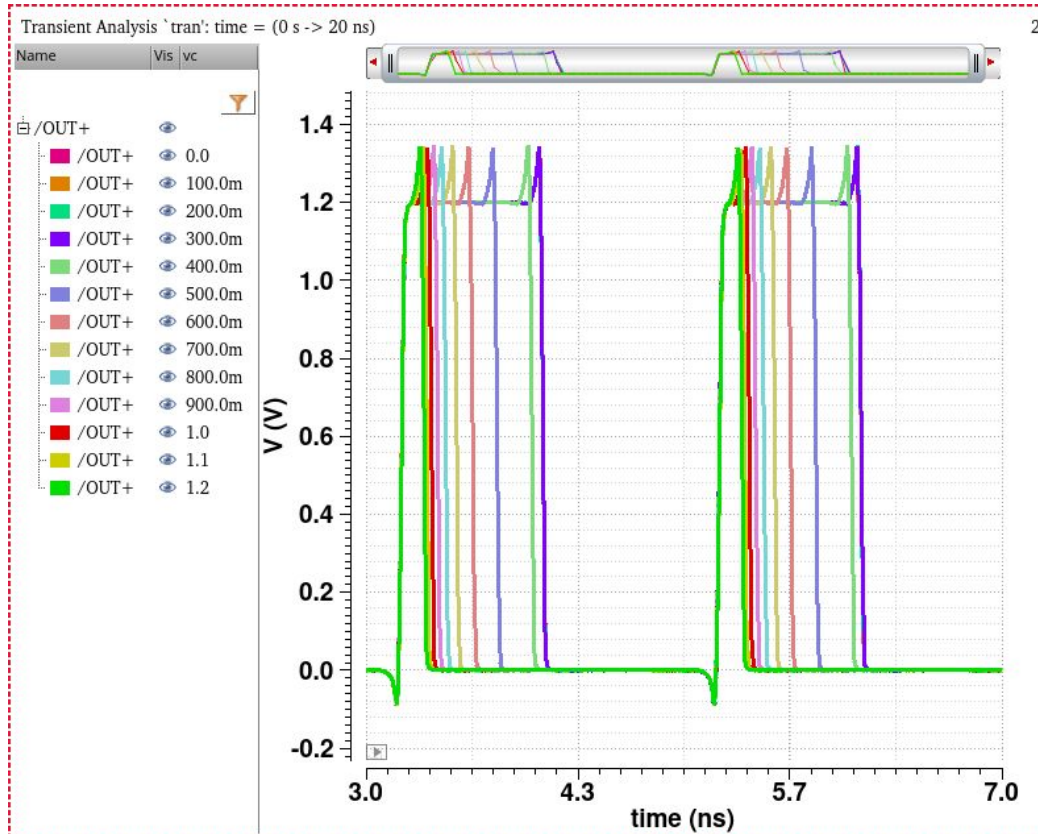


Figure 1: Schematic of a pulse width modulator of a dynamic range of 0% to 50%.

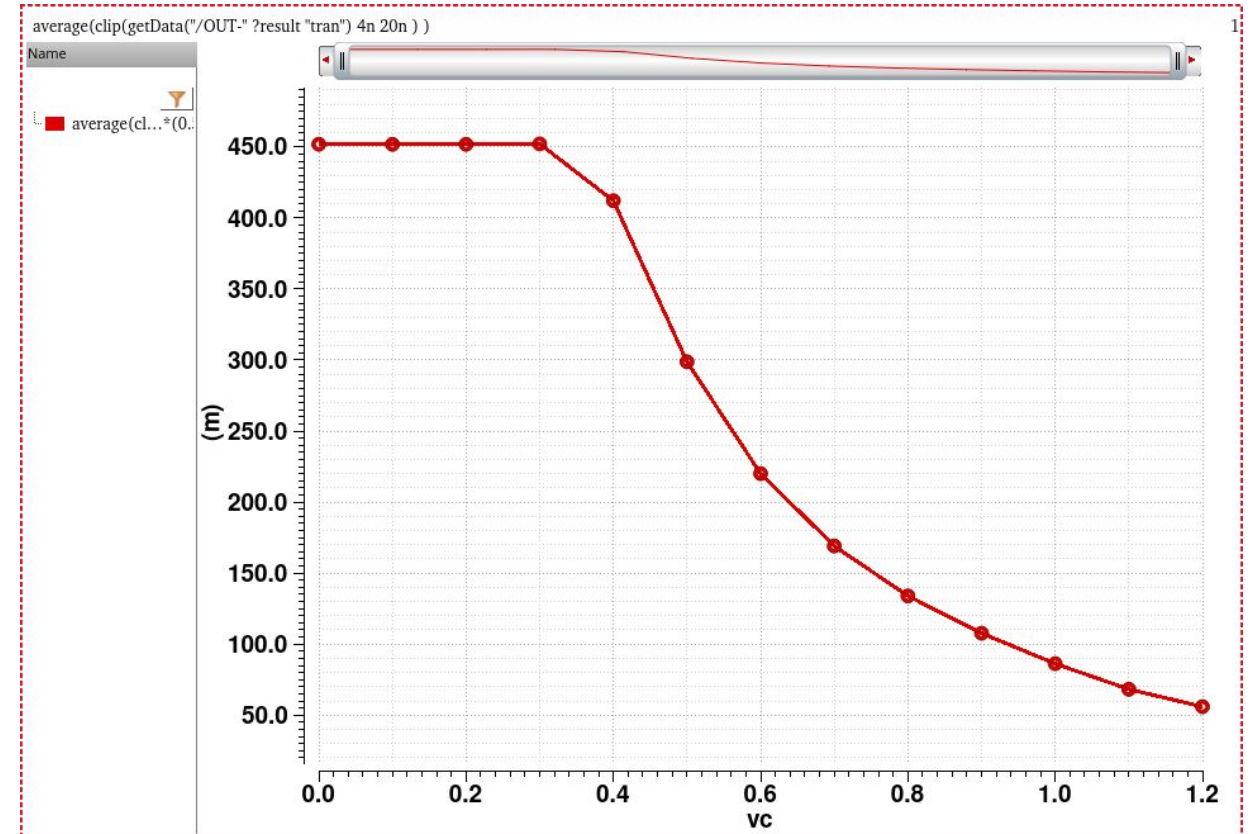


DCM simulation results @500 MHz

- Adequate duty cycle control range (0.45 to 0.05) for a control voltage range of 0.3-1.2 V



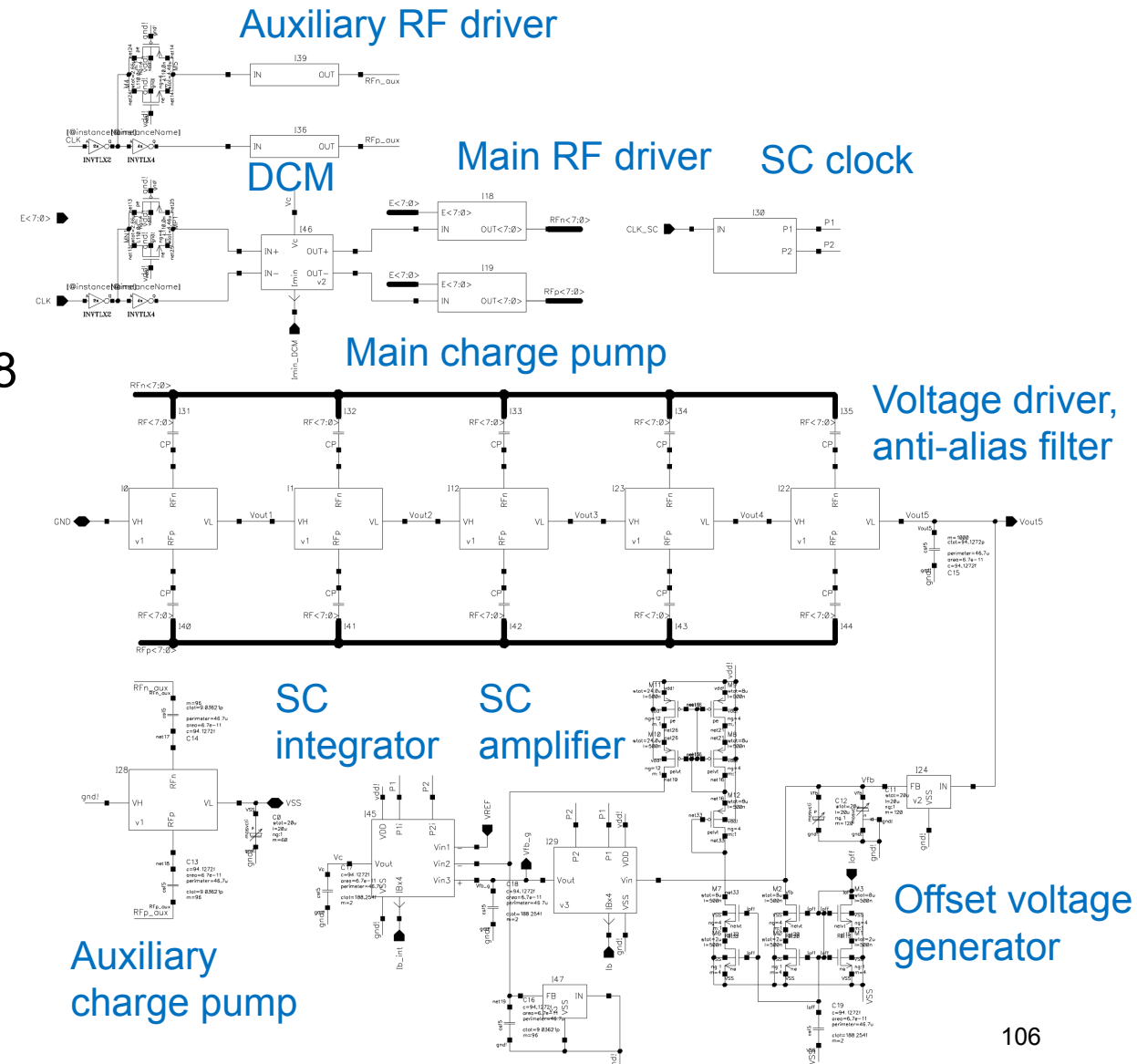
Time-domain waveforms versus control voltage, V_c



Estimated duty cycle versus V_c

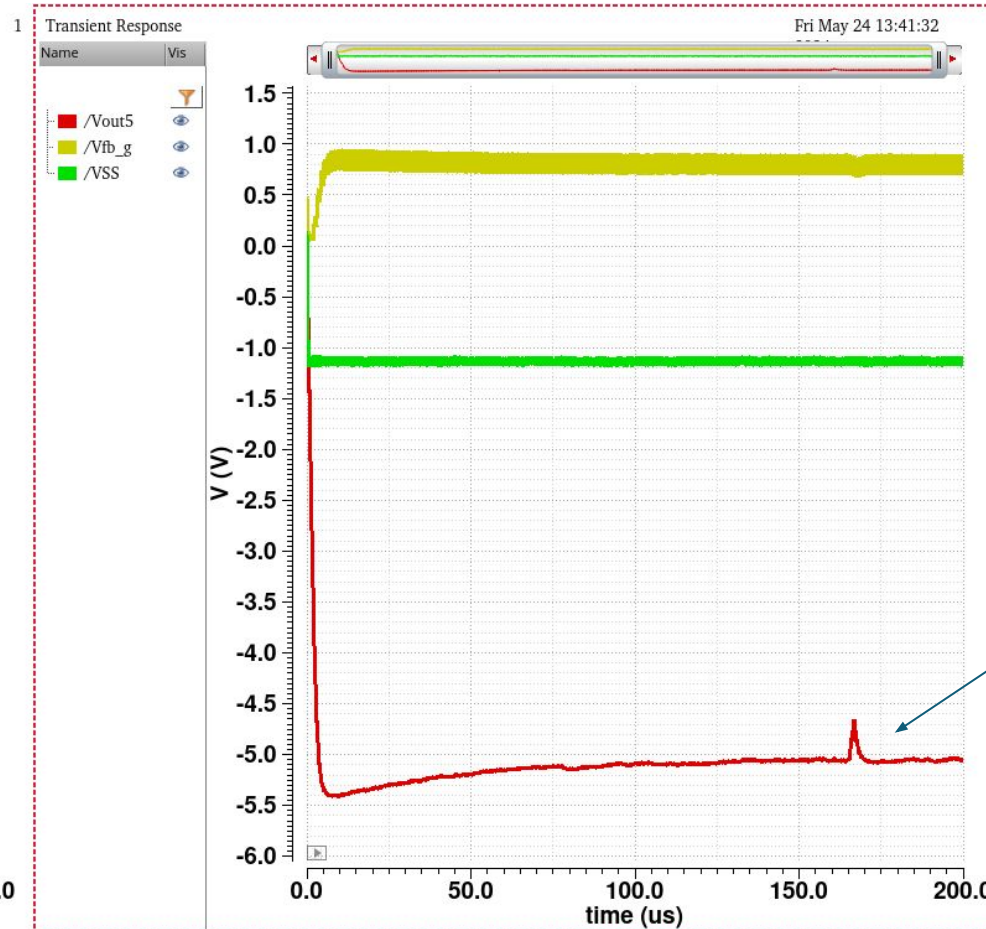
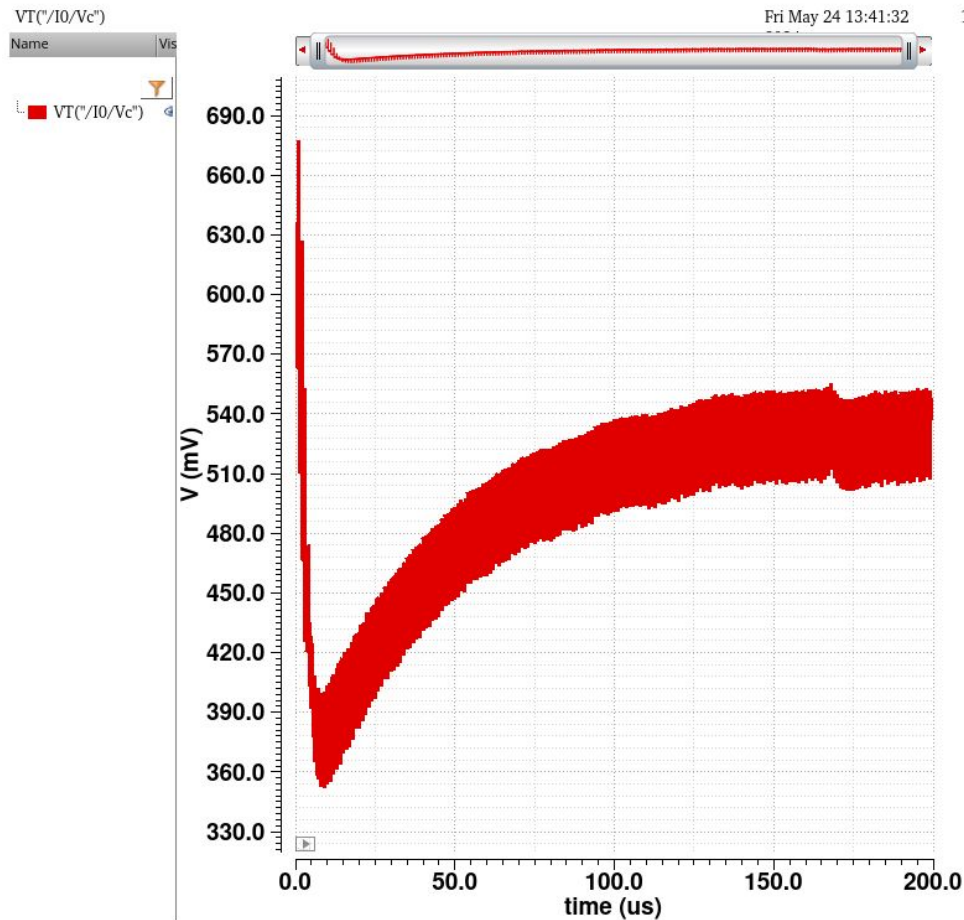
Closed-loop regulator with DCM

- Integrator added in the feedback path to set the control voltage, V_c , of the DCM
- Duty cycle of the auxiliary charge pump is kept fixed at 50% since its output voltage does not need to be adjusted
- RF driver and pump capacitors are split into 8 identical branches
 - Provides coarse control over the output voltage, thus reducing the required control range of the feedback loop
 - Thermometer coding also provides robustness to single-event upsets
- Nominal values:
 - RF frequency = 500 MHz
 - SC clock frequency = 1 MHz



Simulation of the closed-loop regulator

- $V_{REF} = 5 \times (3/20) \text{ V} = 0.75 \text{ V}$, should produce -5V



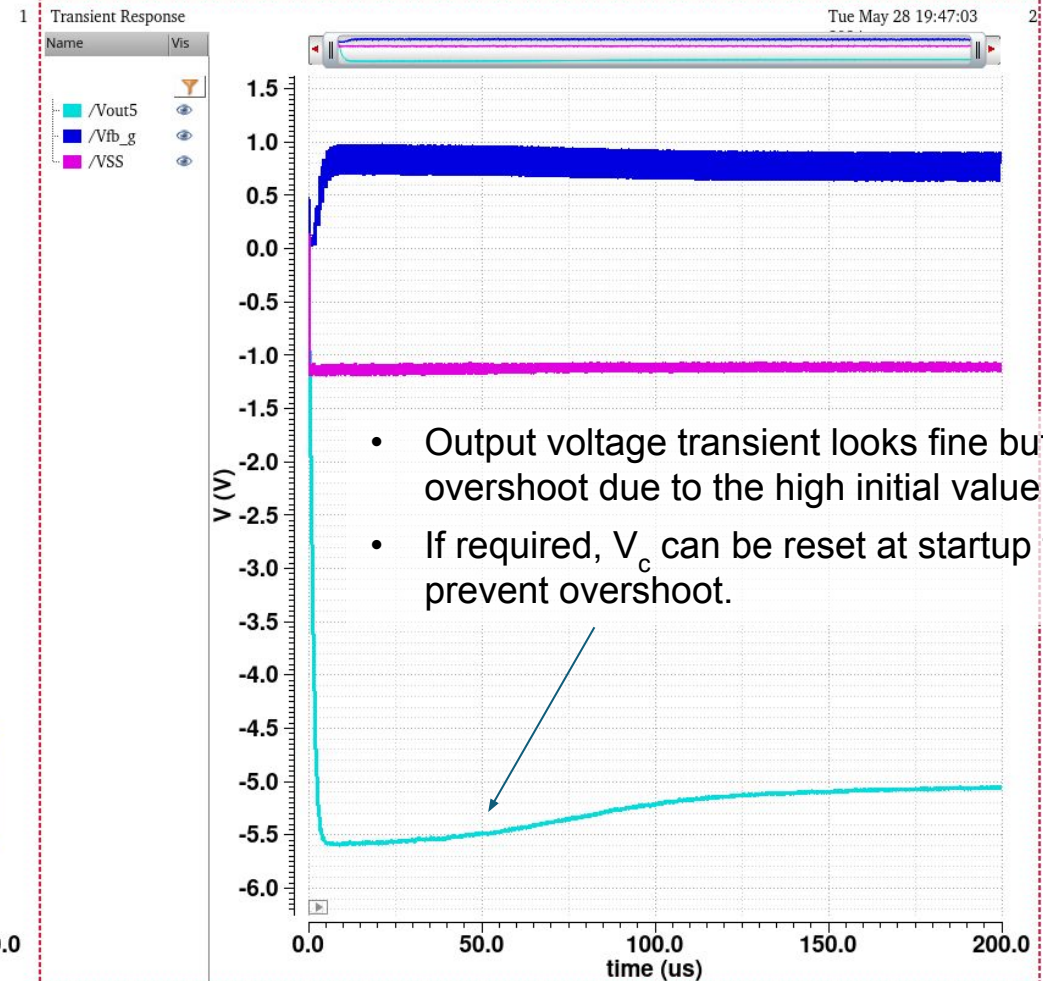
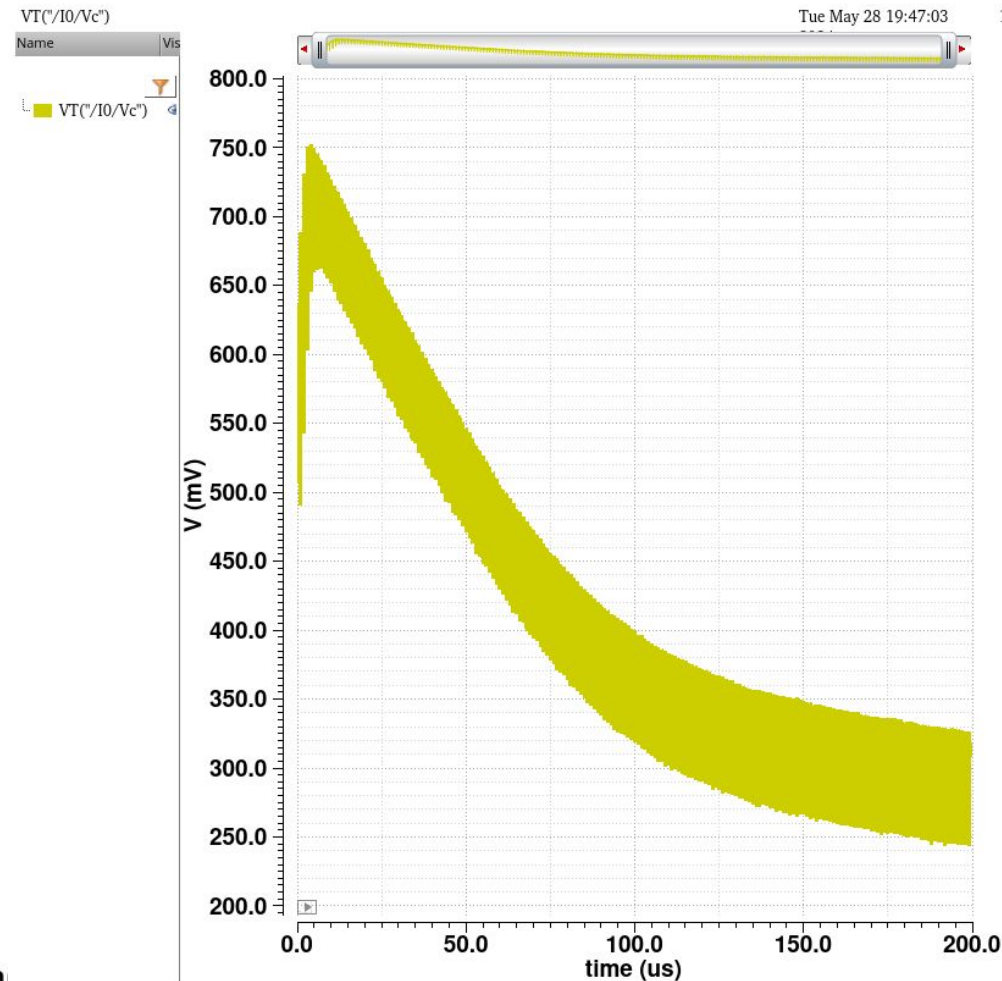
Output voltage transient looks OK, but what's this?

Simulation of the closed-loop regulator

- Further simulations show that the “glitch” often reappears, resulting in slow oscillations in the output voltage
- Hard to stabilize the loop to get rid of these oscillations → simply reducing the bandwidth by increasing the integrator time constant does not work
- It is possible that the oscillations are a simulation artifact, particularly since APS++ frequently has convergence issues on high accuracy settings with the XT011 device models
 - Spectre does not have convergence issues, but is practically unusable for these simulations since it is single-threaded and thus runs about 20x slower
 - On the other hand, it is also possible that these oscillations are real, in which case we should consider a different feedback variable. [What about frequency?](#)

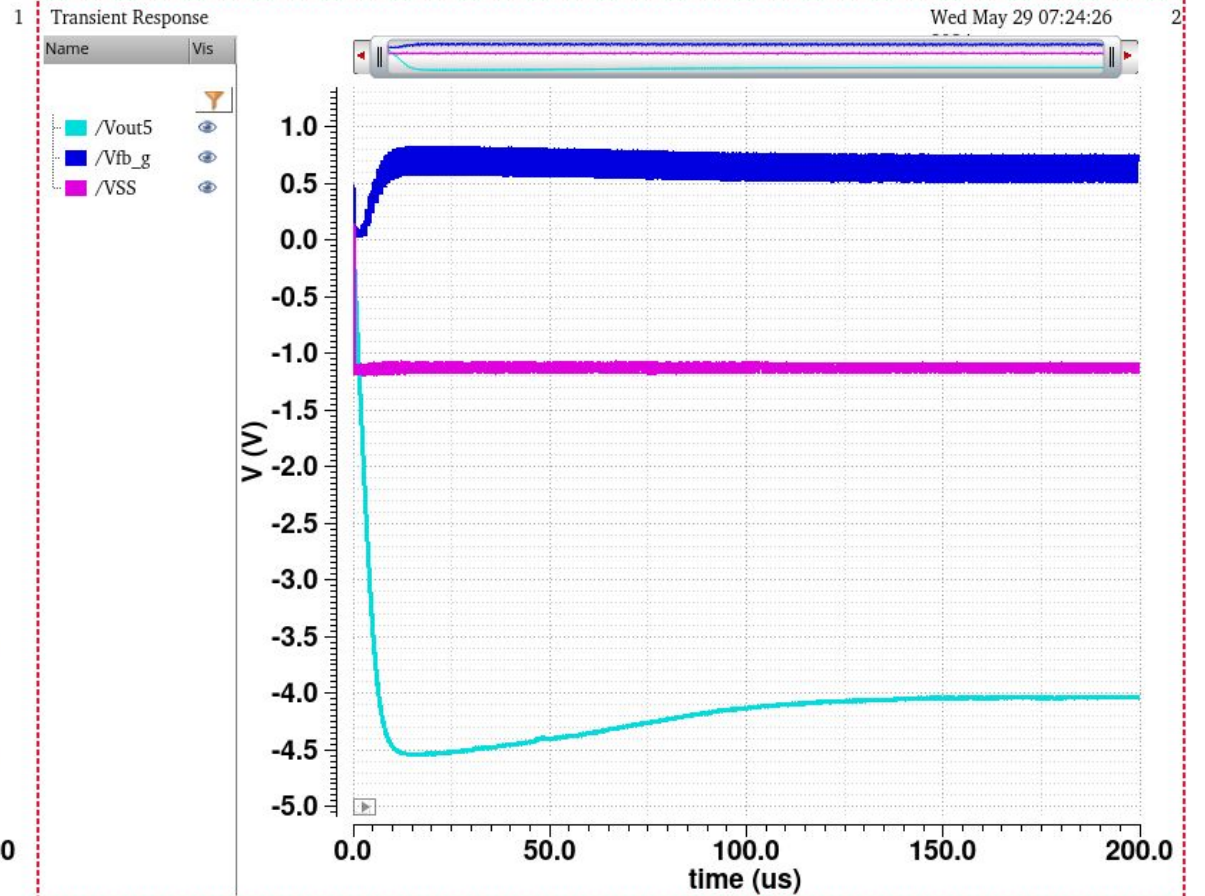
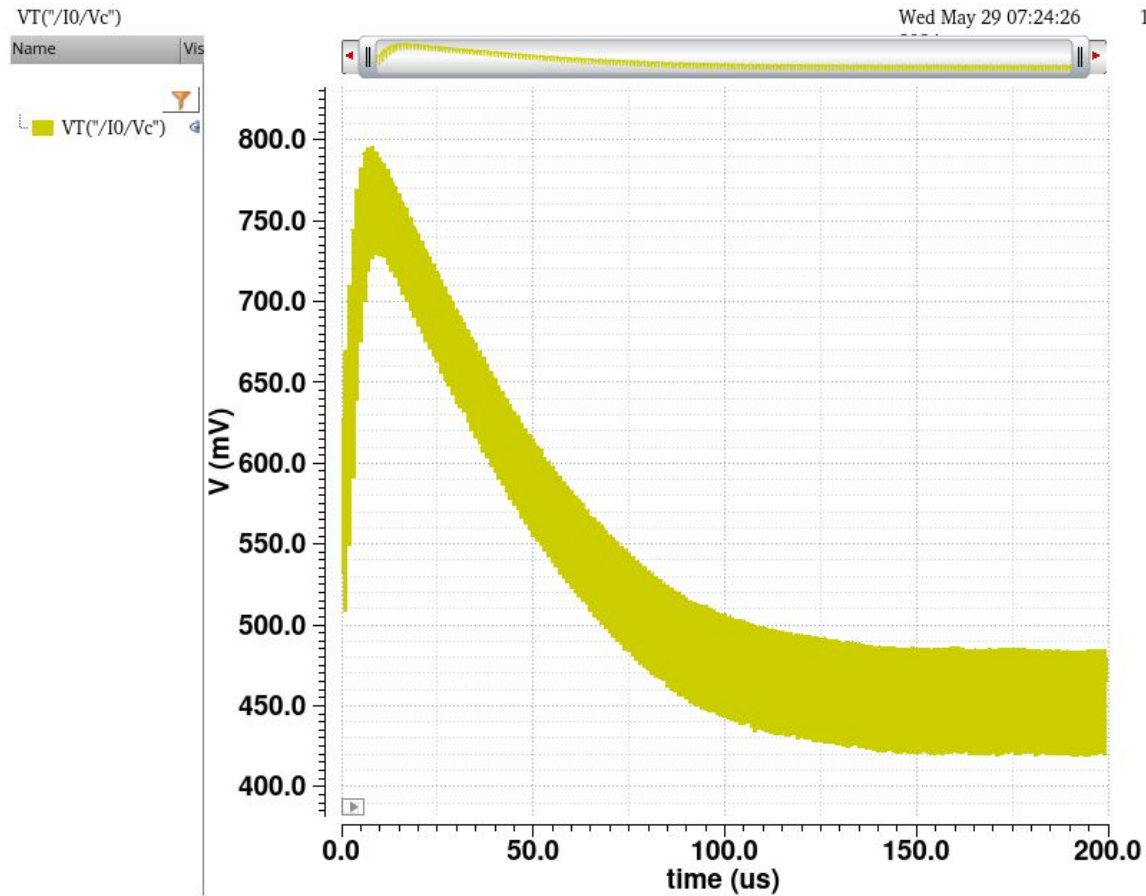
Simulation of the closed-loop regulator

- Drive strength = 16, $V_{REF} = 5 \times (3/20) \text{ V} = 0.75 \text{ V}$, should produce -5V , $R_L = 25 \text{ k}\Omega$



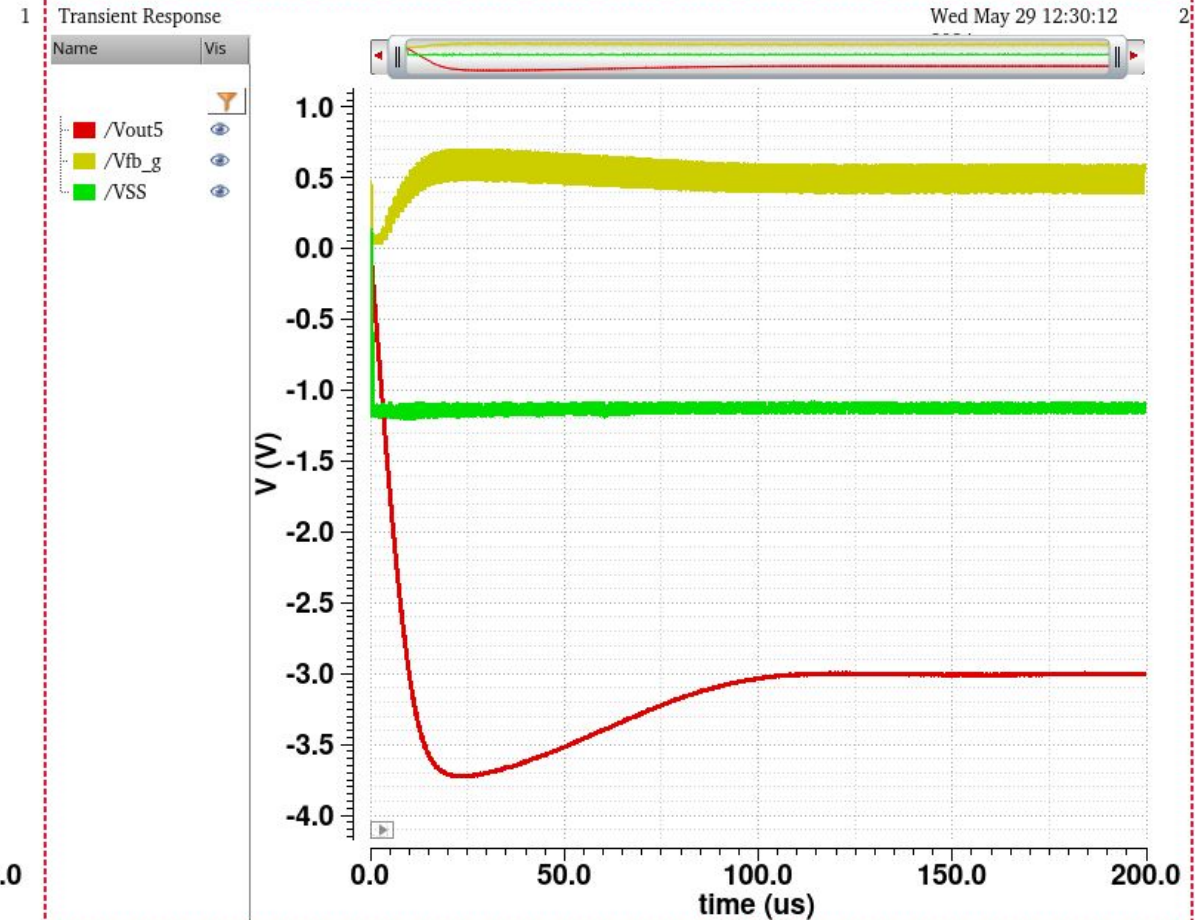
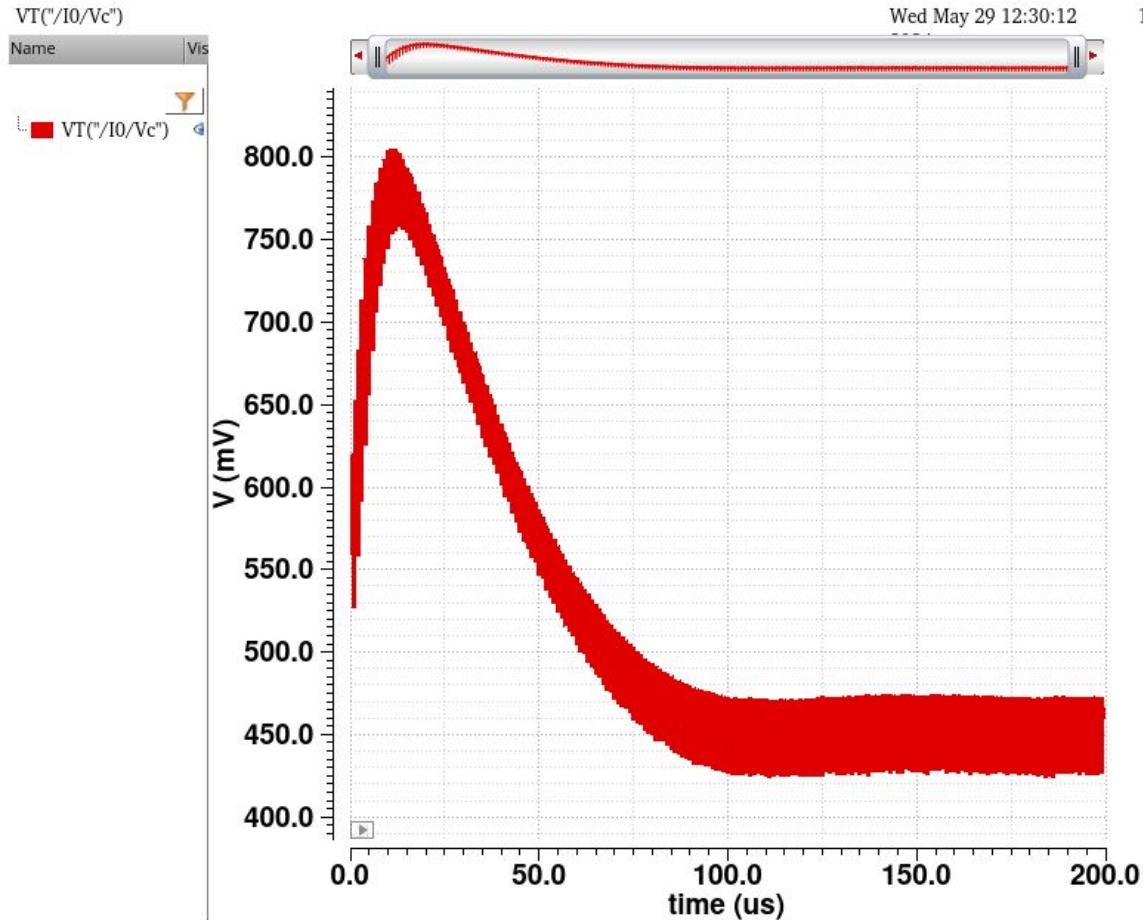
Simulation of the closed-loop regulator

- Drive strength = 4, $V_{REF} = 4 \times (3/20) \text{ V} = 0.6 \text{ V}$, should produce -4V , $R_L = 25 \text{ k}\Omega$



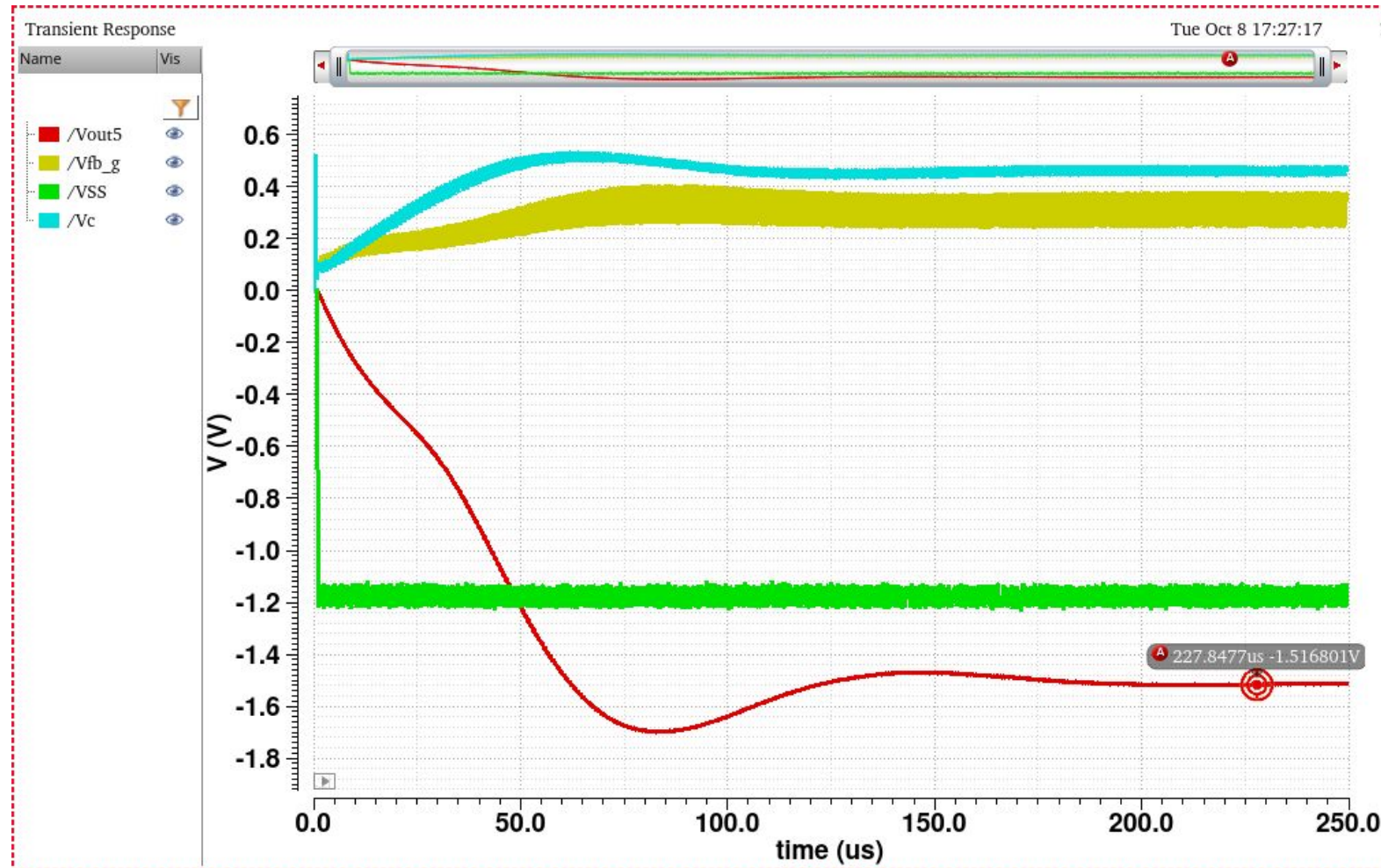
Simulation of the closed-loop regulator

- Drive strength = 2, $V_{REF} = 3 \times (3/20) \text{ V} = 0.45 \text{ V}$, should produce -3V , $R_L = 25 \text{ k}\Omega$



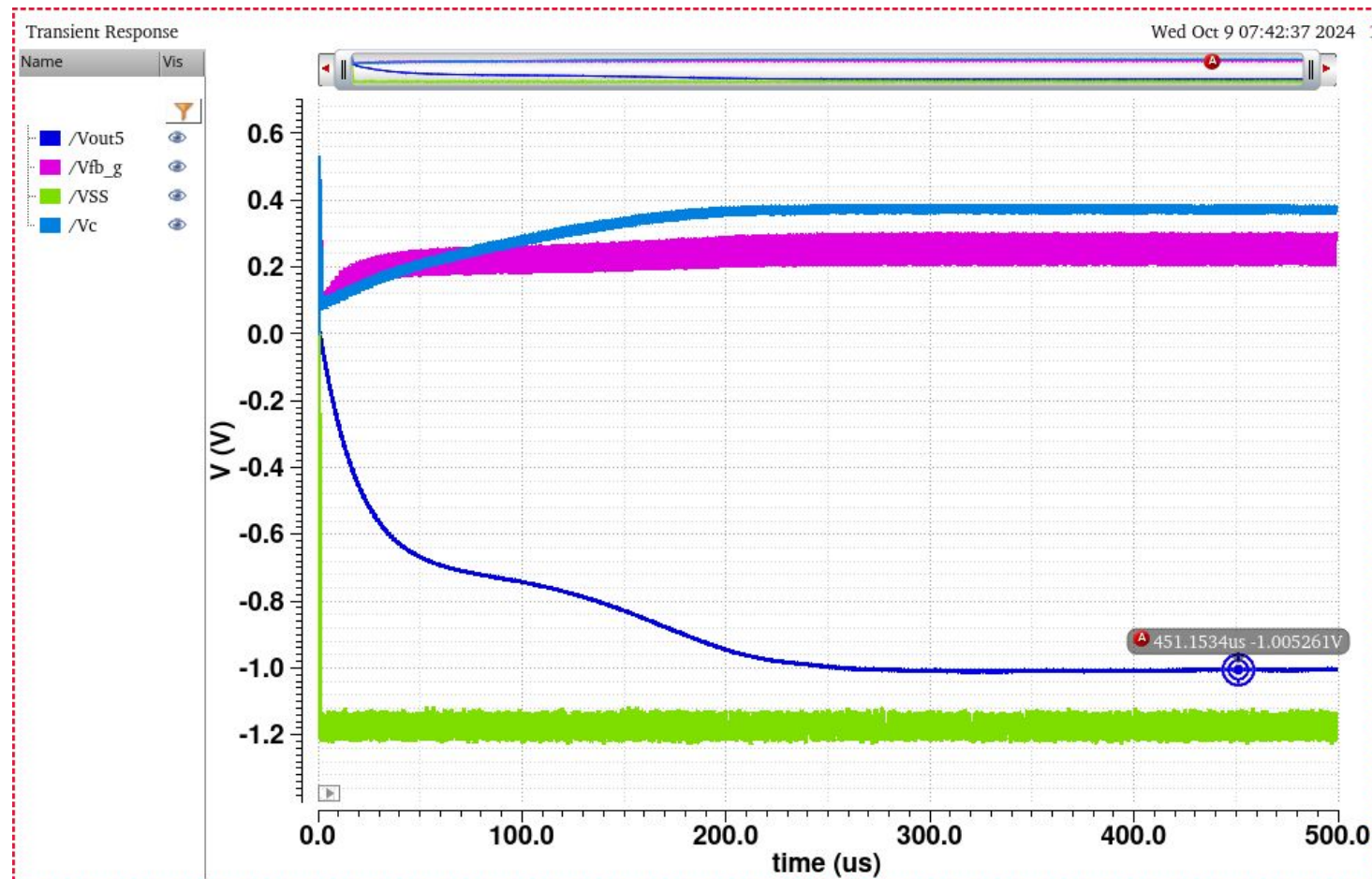
Simulation of the closed-loop regulator

- Drive strength = 1, $V_{REF} = 1.5 \times (3/20) \text{ V} = 0.225 \text{ V}$, should produce -1.5V , $R_L = 25 \text{ k}\Omega$



Simulation of the closed-loop regulator

- Drive strength = 1, $V_{REF} = 1 \times (3/20) \text{ V} = 0.15 \text{ V}$, should produce -1V , $R_L = 25 \text{ k}\Omega$
- SC clock frequency was reduced by 2x (to 500 kHz) to reduce loop bandwidth and thus improve the phase margin



Corner simulations

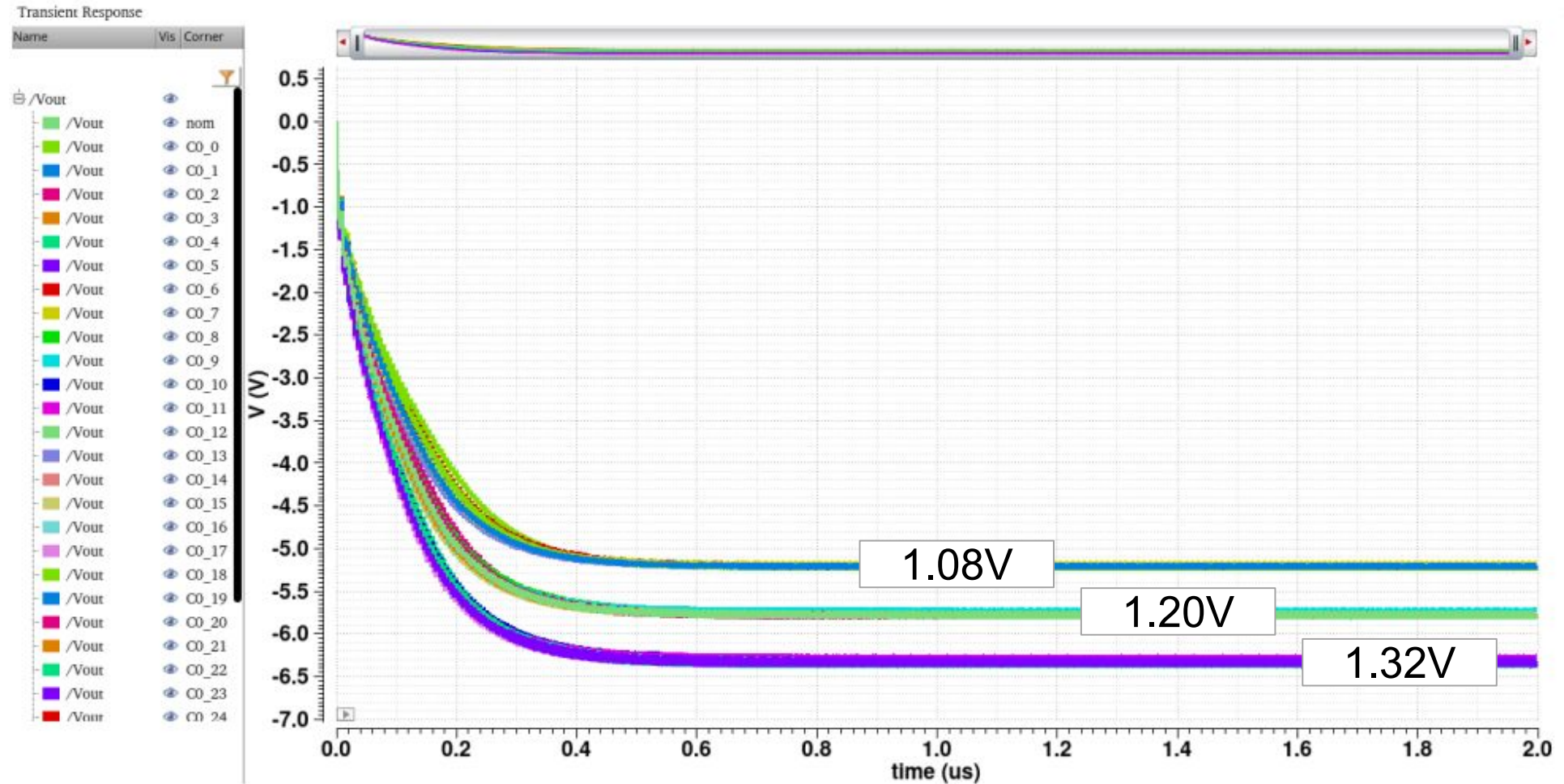
- X-FAB design kits include the following model variants:

- tm - typical mean - middle of process tolerances
- wp - worst case power (fast) V_t min, I_d max, R_{min} , C_{min}
- ws - worst case speed (slow) V_t max, I_d min, R_{max} , C_{max}
- wo - worst case one (R_{on} NMOS_{min}, R_{on} PMOS_{max})
- wz - worst case zero (R_{on} NMOS_{max}, R_{on} PMOS_{min})

- PVT corners:

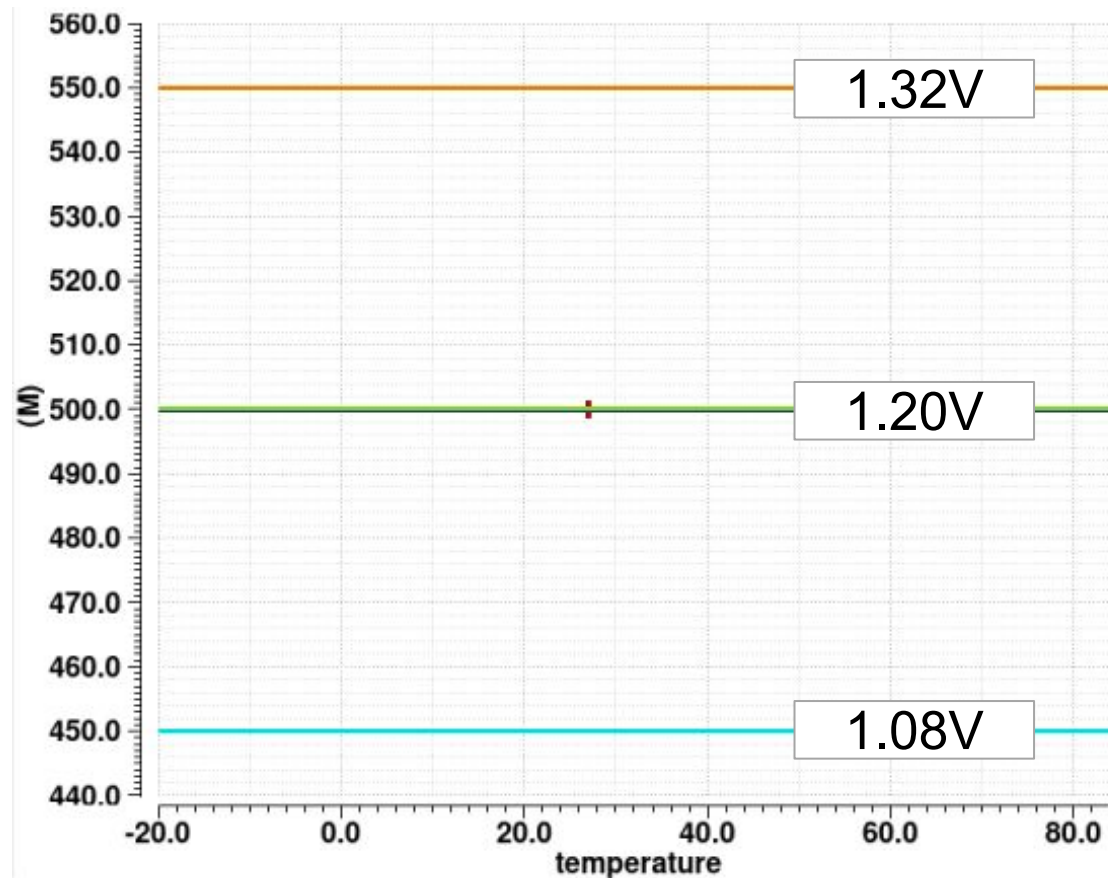
- MOS: tm, wp, ws, wo, wz
- CAP: tm, wp, ws
- Temp: -20C, +85C
- Supply: 1.08 V, 1.2 V, 1.32 V

Corner simulations (open-loop charge pump)



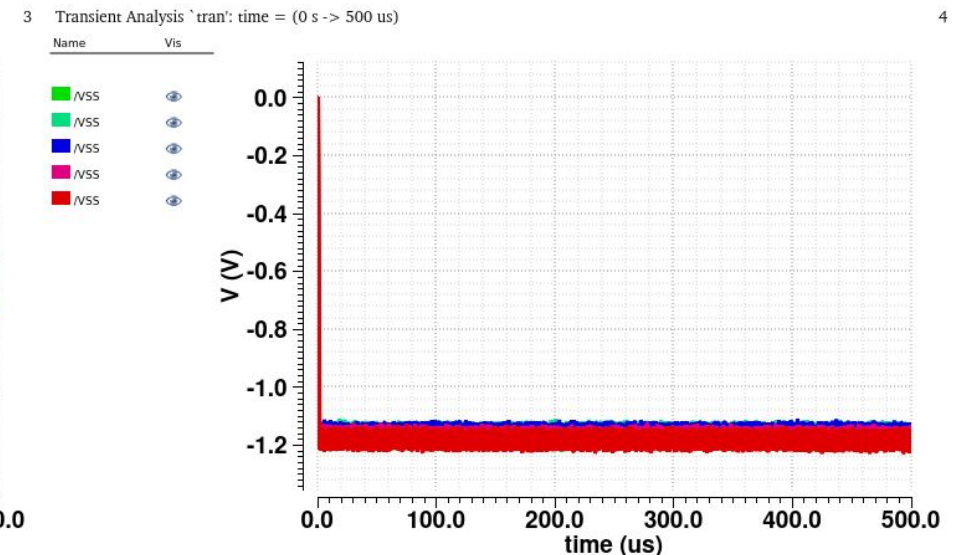
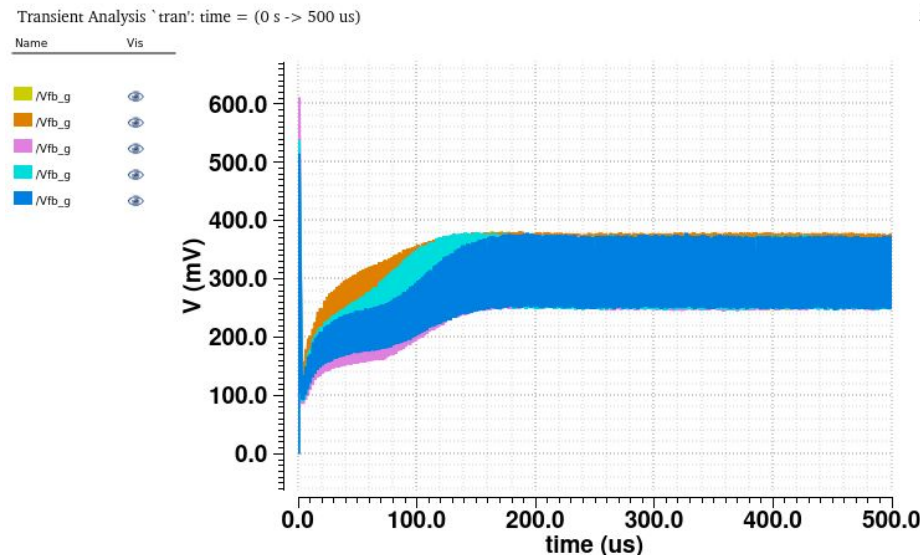
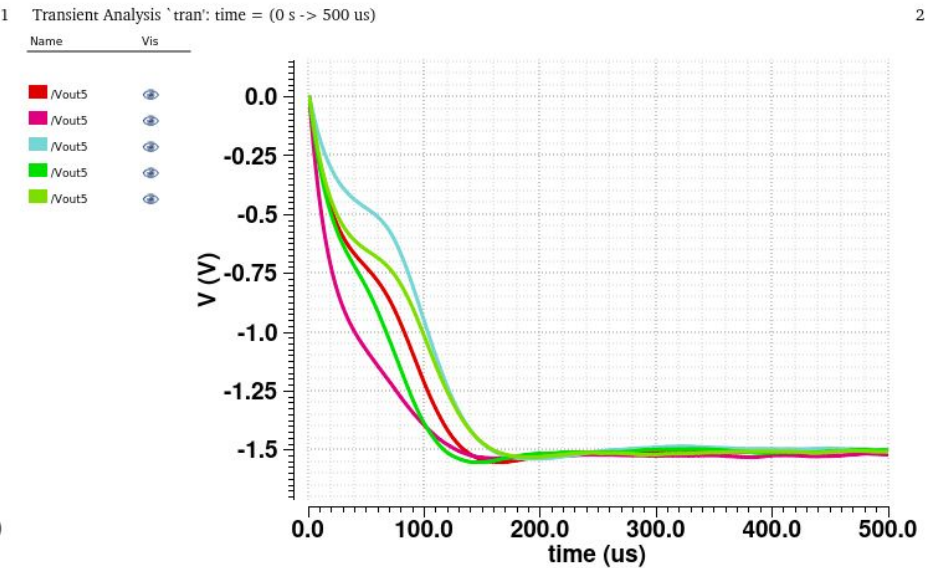
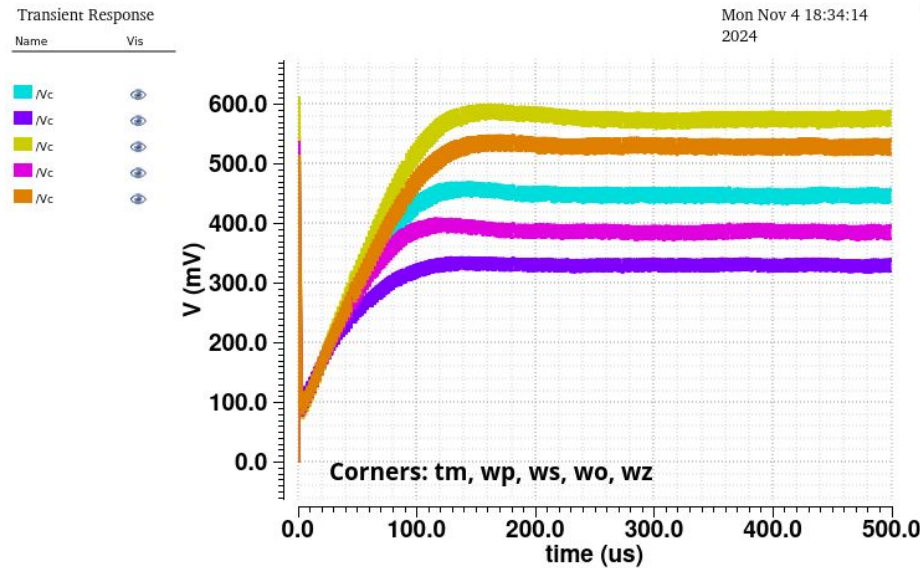
Corner simulations (RF driver)

- Nominal RF frequency: 500 MHz



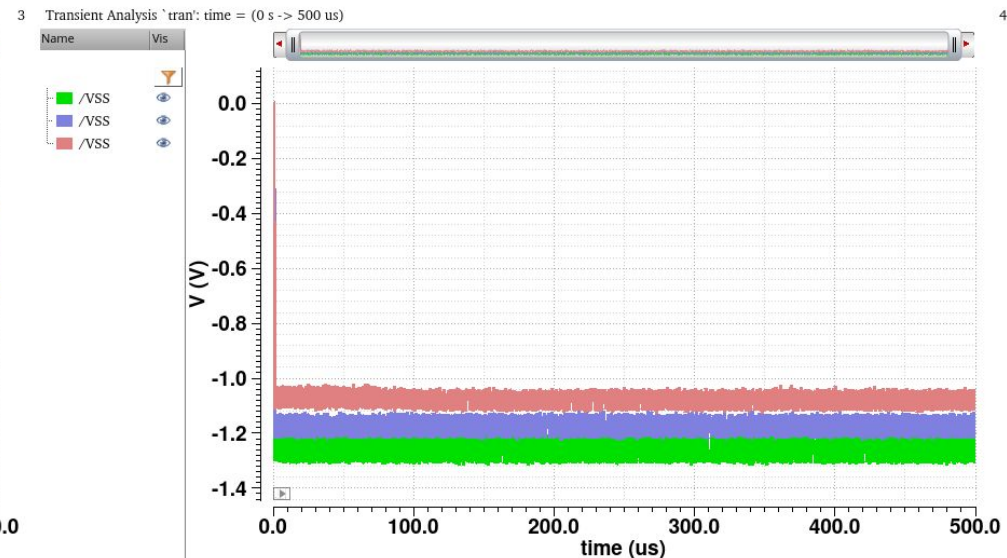
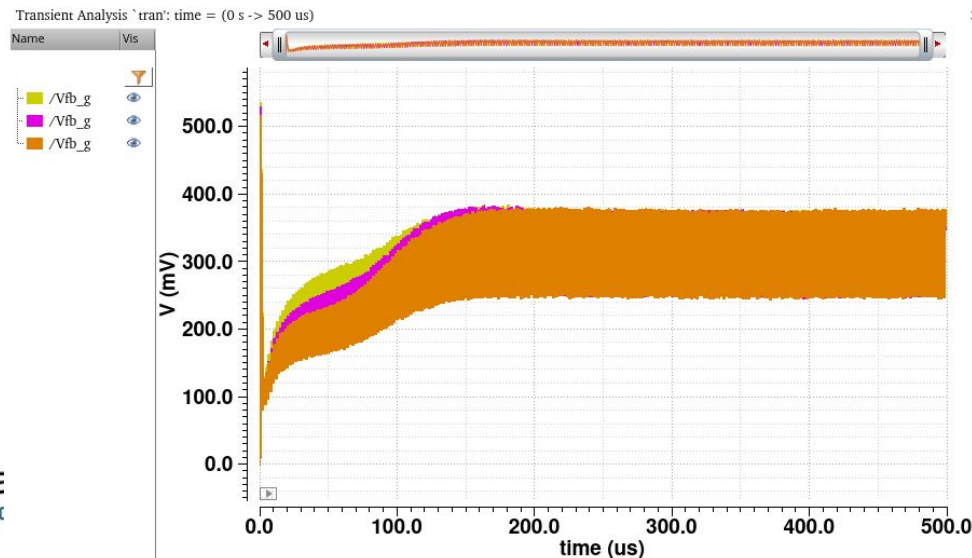
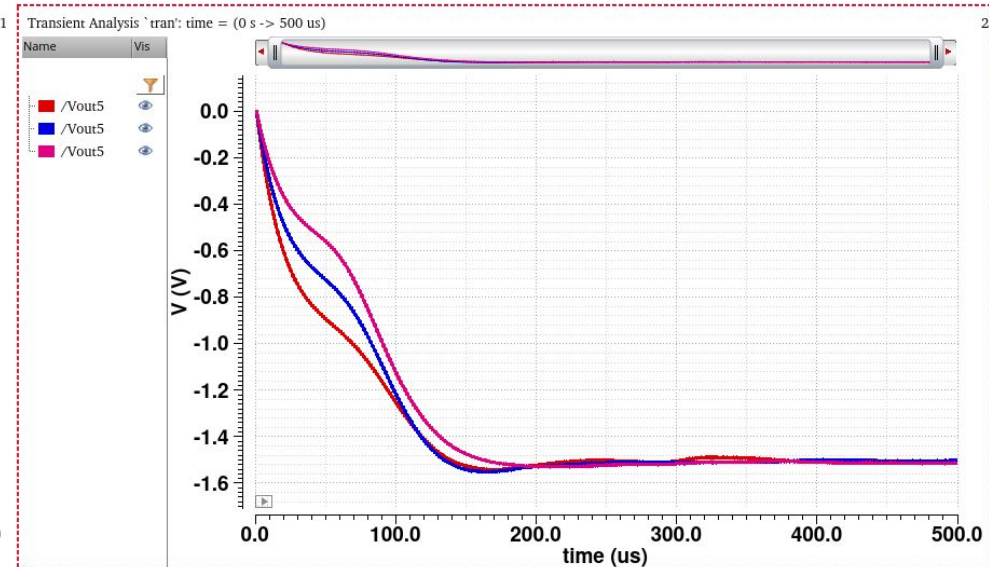
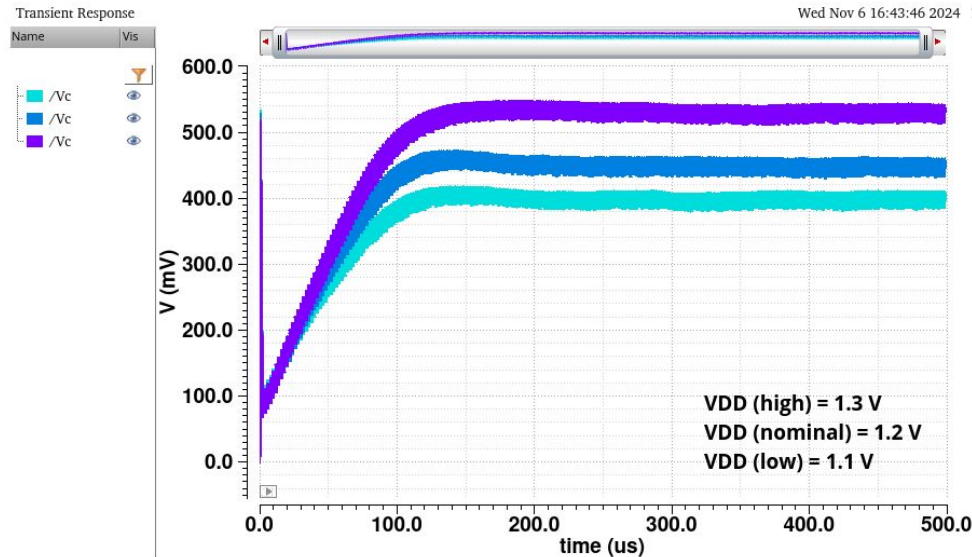
Corner simulations (complete regulator)

- Desired output voltage = -1.5 V, $R_L = 25\text{ k}\Omega$



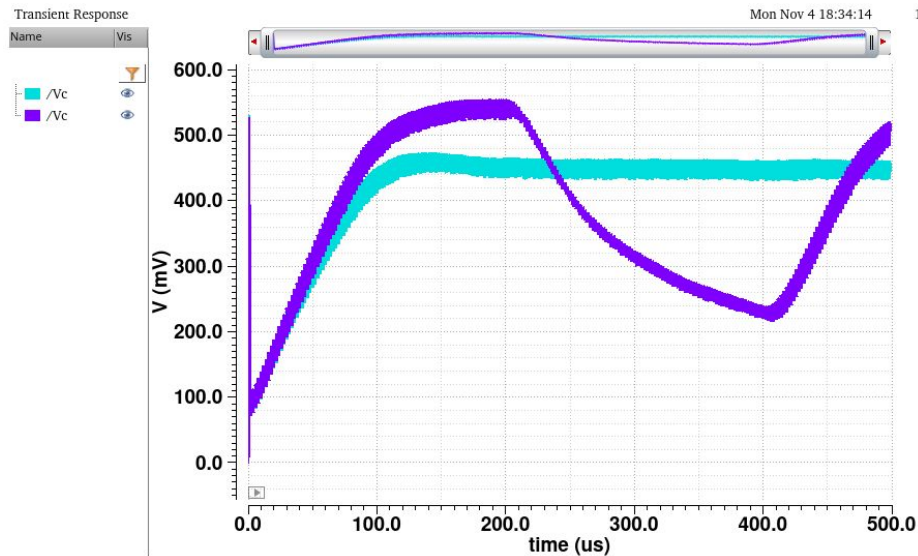
Corner simulations (complete regulator)

- Desired output voltage = -1.5 V, $R_L = 25\text{ k}\Omega$



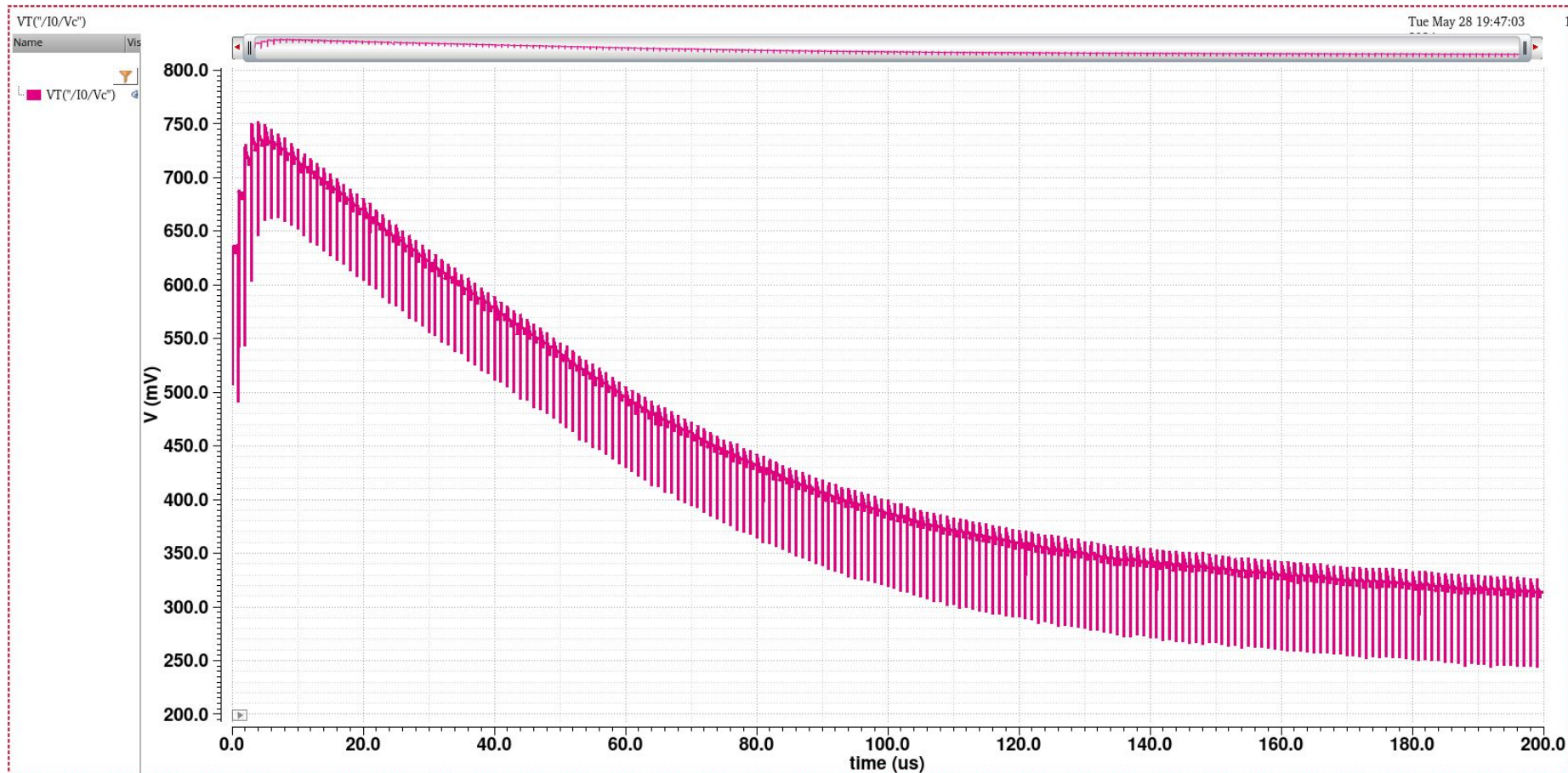
Load response (complete regulator)

- Desired output voltage = -1.5 V, nominal $R_L = 15\text{ k}\Omega$



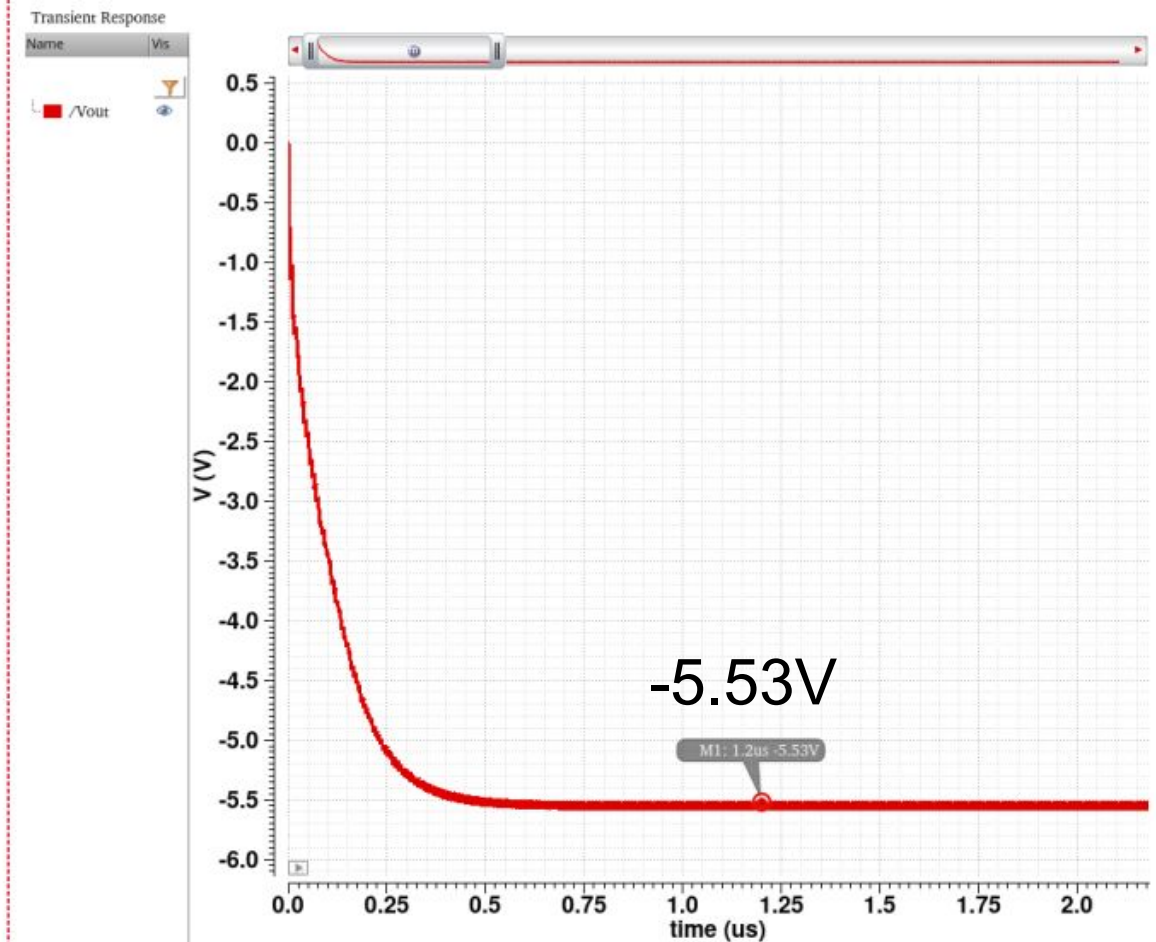
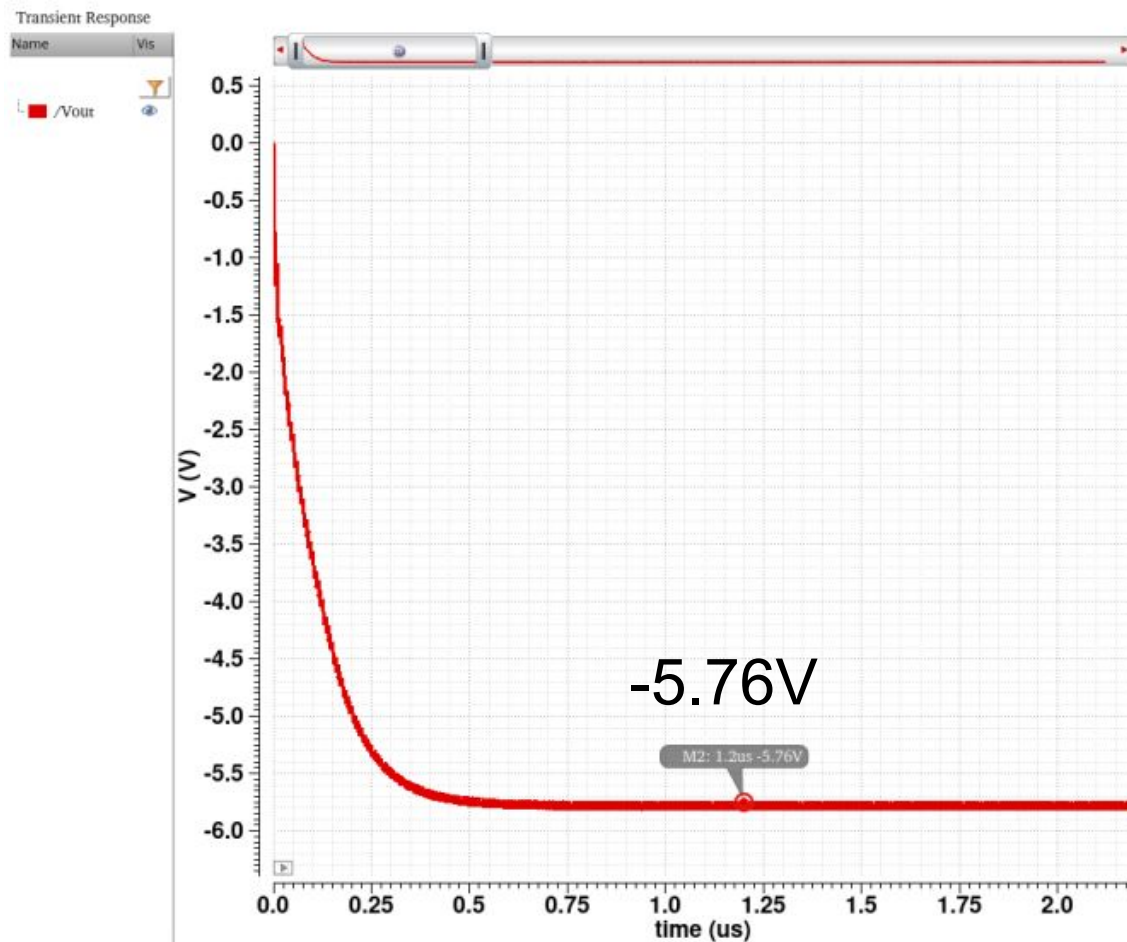
Simulation of the closed-loop regulator

- Drive strength = 16, $V_{REF} = 5 \times (3/20) \text{ V} = 0.75 \text{ V}$, should produce -5V
- Detail of the integrator output, i.e., the VCO control voltage



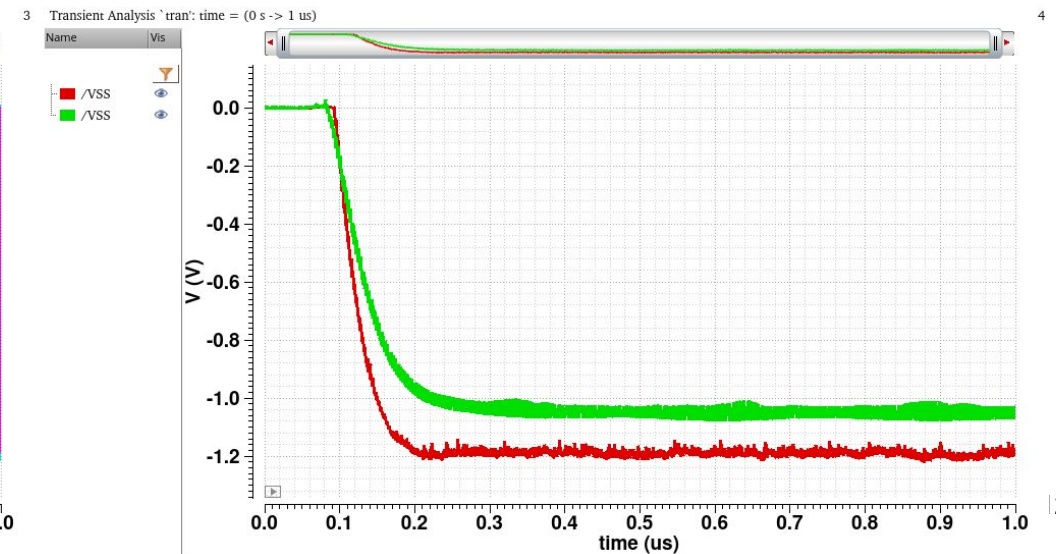
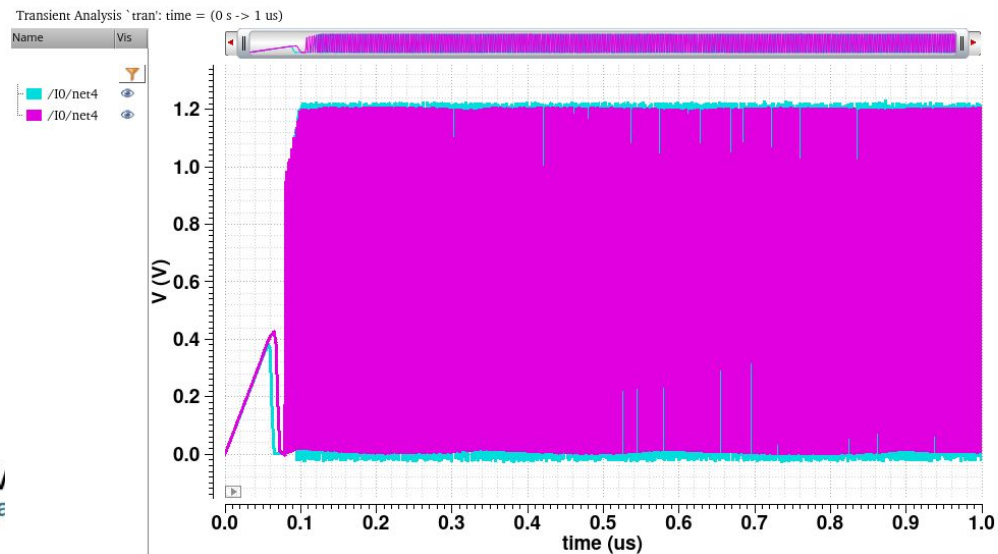
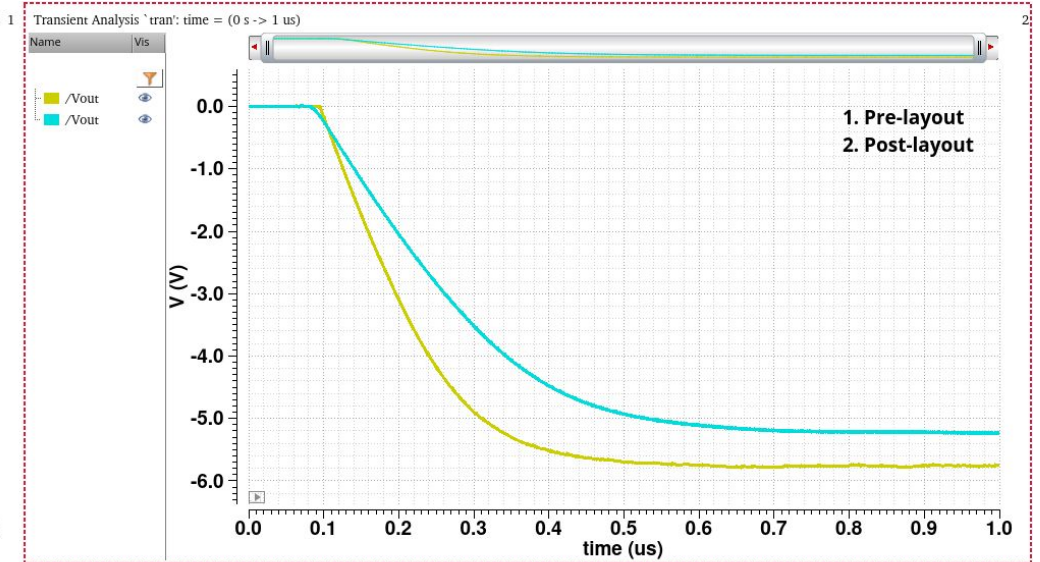
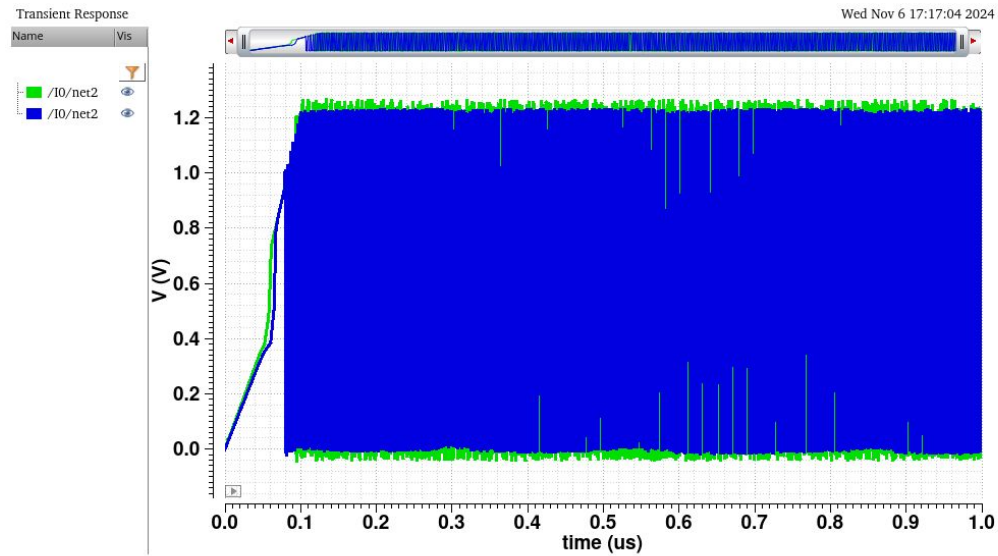
Pre and post-layout simulations

- Open-loop charge pump, no load



Pre and post-layout simulations

- Open-loop charge pump, no load

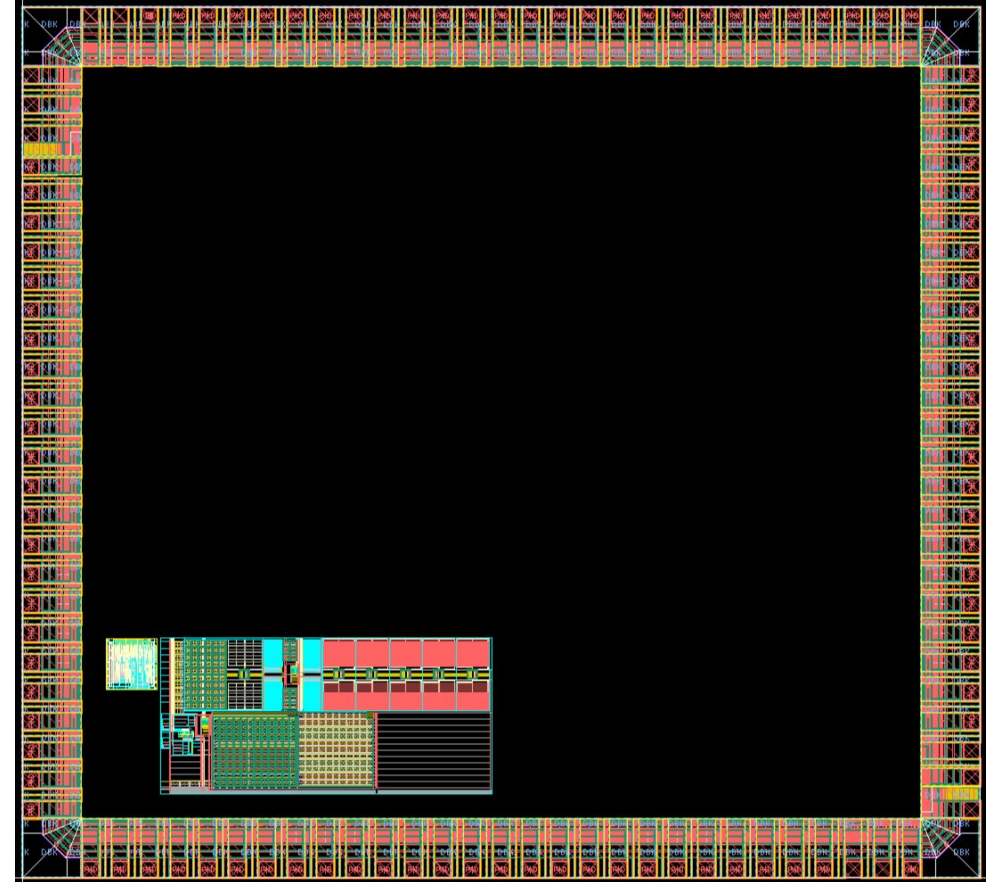
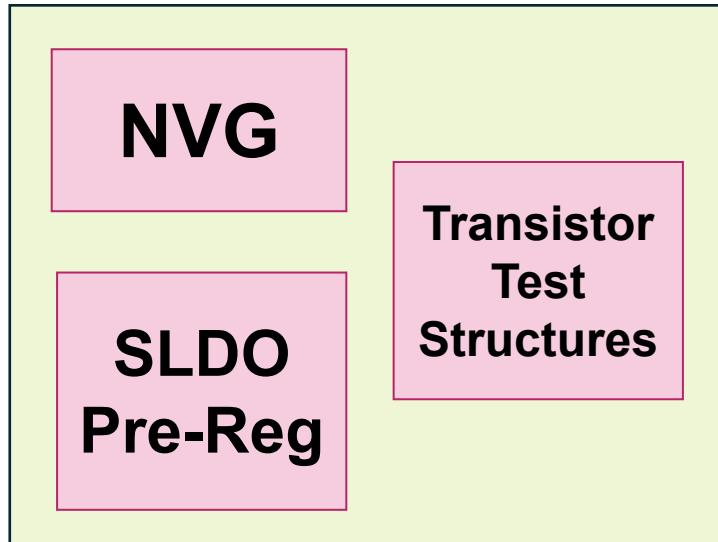


Pre and post-layout simulations (complete regulator)

- Desired output voltage = -1.5 V, $R_L = 25 \text{ k}\Omega$
- Simulation does not converge – being studied.

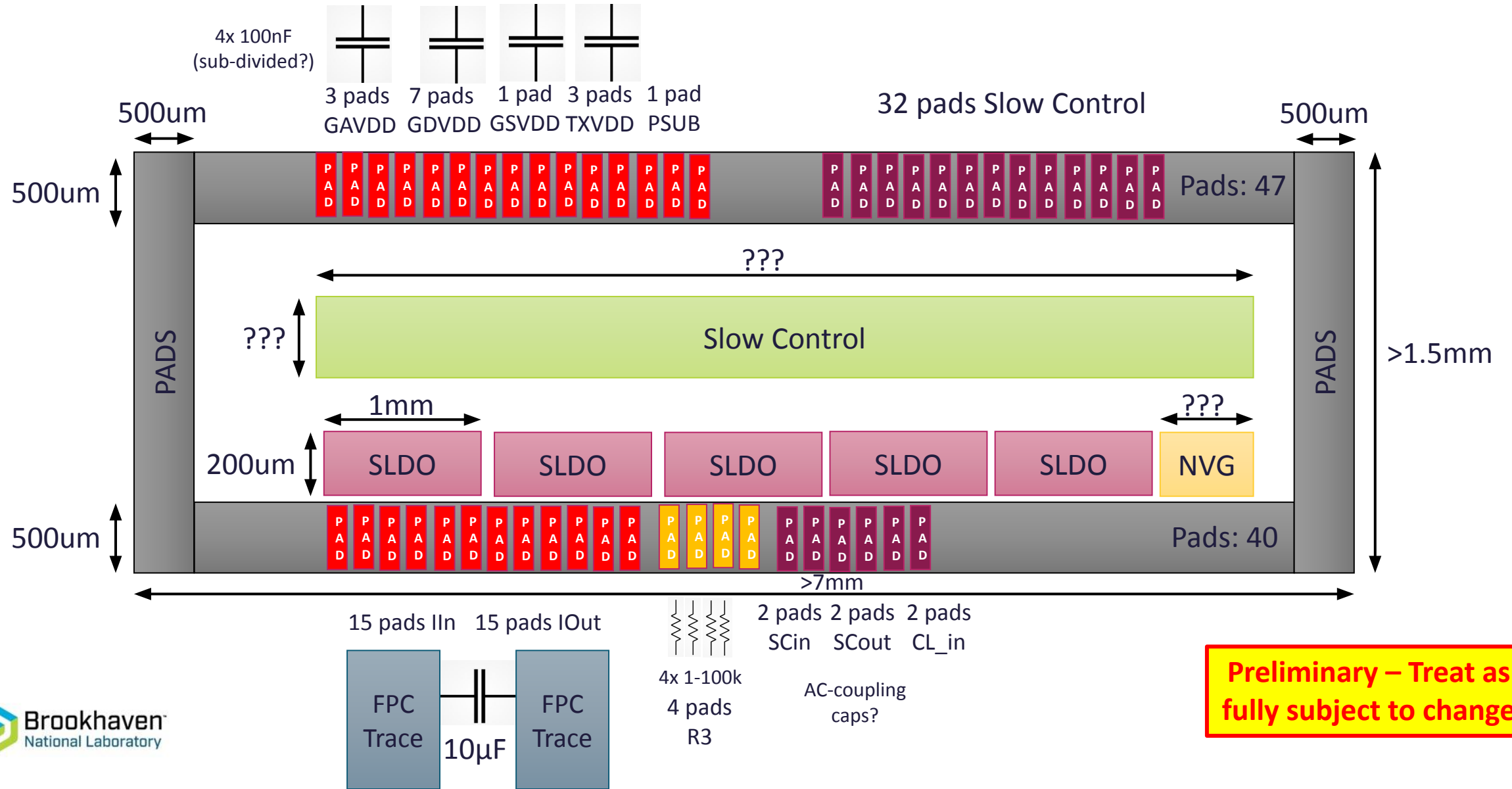
Design of MPW1

- **Contents:**
 - Negative voltage generator (NVG)
 - SLDO pre-regulator
 - Transistor test structures
- Number of available pads = $2 \times (29 + 26) = 110$
- Pad pitch = $100\text{ }\mu\text{m}$
- Tapeout planned in November 2024



Size = $3264\text{ }\mu\text{m} \times 2964\text{ }\mu\text{m} = 9.675\text{ mm}^2$

AncASIC Size and Pads



Future work

- Replace the regular switched-capacitor integrator with a CDS version to eliminate offset and gain errors
- Design a voltage DAC to generate the reference voltage, V_{REF} , thus allowing the output voltage to be digitally programmed.
- Model and simulate impact of single-event transients.
- If needed, use enclosed layout transistors (ELTs) to improve TID tolerance.